PY32F003 Datasheet

32-bit ARM® Cortex®-M0+ Microcontroller

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Features

- Core
  - — 32-bit ARM® Cortex® - M0+ CPU
  - — Up to 32 MHz operating frequency
- Memories
  - — Maximum 64 Kbytes of flash memory
  - — Up to 8 Kbytes SRAM
- Clock system
  - — Internal 4/8/16/ 22.12/24 MHz RC Oscillator (HSI)
  - — Internal 32.768 kHz RC oscillator (LSI)
  - — 4 to 32 MHz crystal oscillator (HSE)
- Power management and reset
  - — Operating voltage(x6 version): 1.7 ~ 5.5 V
  - — Operating voltage(x7 version): 2.0 ~ 5.5 V
  - — Low power modes: Sleep and Stop
  - — Power-on/Power-down reset (POR/PDR)
  - — Brownout Detect Reset (BOR)
  - — Programmable Voltage Detection (PVD)
- General purpose input and output (I/O)
  - — Up to 18 I/Os, all available as external interrupts
  - — Driver current 8mA
- 3-channel DMA controller
- 1 x 12-bit ADC
  - — Supports up to 10 external input channels
  - — Input voltage conversion range: 0 ~ V_{CC}
- Timer
  - — A 16bit advanced control timer (TIM1)
  - — 4 general purpose 16-bit timers (TIM3/TIM14/TIM16/TIM17)
  - — A low-power timer (LPTIM), supports wake-up from Stop mode
  - — An Independent Watchdog Timer (IWDT)
  - — A Window Watchdog Timer (WWDT)
  - — A SysTick timer
  - — A IRTIM
- RTC
- Communication Interface
  - — A Serial Peripheral Interface (SPI)
  - — Two Universal Synchronous / Asynchronous Transceivers (USARTs) with automatic baud-rate detection
  - — A I^2C interface , supports standard mode (100 kHz) , Fast mode (400 kHz) , supports 7-bit addressing mode
- Hardware CRC-32 module
- Two comparators
- Unique UID
- Serial wire debug (SWD)
- Operating temp. (x6 version): -40 ~ 85 ℃
- Operating temp. (x7 version): -40 ~ 105 ℃
- Package: TSSOP20,QFN20,SOP20,SOP16, MSOP10,SOP8, DFN8(3*2)

Contents

1. Introduction

PY32F003 series microcontrollers are MCUs with high performance 32-bit ARM® Cortex® -M0 + core, wide voltage operating range. It has embedded up to 64 Kbytes flash and 8 Kbytes SRAM memory, a maximum operating frequency of 32 MHz, and contains various products in different package types. The chip integrates multi-channel I^2C, SPI, USART and other communication peripherals, one channel 12bit ADC, five 16bit timers, and two-channel comparators.

PY32F003 series microcontrollers are -40 ~ 85 ℃ and -40 ~ 105 ℃, the operating voltage range are 1.7 ~ 5.5 V and 2.0 ~ 5.5 V. The chip provides sleep and stop low-power operating modes from meeting different low-power applications.

The PY32F003 series of microcontrollers are suitable for various application scenarios, such as controllers, portable devices, PC peripherals, gaming and GPS platforms, industrial applications.

Table 1-1 PY32F003x6 series TSSOP20 product features and peripheral counts

Peripherals		PY32F003 F18P6	PY32F003 F18P6-E	PY32F003 F16P6	PY32F003 F16P6-E	PY32F003 F14P6	PY32F003 F26P6	PY32F003 F36P6	PY32F003 F48P6	PY32F003 F56P6	PY32F003 F68P6
Flash (Kbytes)		64	64	32	32	16	32	32	64	32	64
SRAM (Kbytes)		8	8	4	4	2	4	4	8	4	8
Timers	Advanced	1 (16-bit)									
	General pupose	4 (16-bit)									
	low power	1									
	SysTick	1									
	Watchdog	2									
Comm. inter-faces	SPI	1									
	I^2C	1									
	USART	2									
DMA		3ch									
RTC		Yes									
GPIOs		18									
12-bit ADC (external + internal)		8+2					9+2	6+2	6+2	7+2	10+2
Comparators		2									
Max. CPU frequency		32 MHz									
Operating Voltage		1.7 ~ 5.5 V									
Operating Temp.		-40 ~ 85 °C									
Package		TSSOP20									

Table 1-2 PY32F003x6 series QFN20/SOP20 product features and peripheral counts

Peripherals		PY32F003F18 U6	PY32F003F17 U6	PY32F003F16 U6	PY32F003F16 U6-E	PY32F003F14 U6	PY32F003F26 U6	PY32F003F18 S6
Flash (Kbytes)		64	48	32	32	16	32	64
SRAM (Kbytes)		8	6	4	4	2	4	8
Timers	Advanced	1 (16-bit)						
	General pupose	4 (16-bit)						
	low power	1						
	SysTick	1						
	Watchdog	2						
Comm. interfaces	SPI	1						
	I^2C	1						
	USART	2						
DMA		3ch						
RTC		Yes						
GPIOs		18						
12-bit ADC (external + internal)		8+2					5+2	10+2
Comparators		2						
Max. CPU frequency		32 MHz						
Operating Voltage		1.7 ~ 5.5 V						
Operating Temperature		-40 ~ 85 °C						
Package		QFN20						SOP20

Table 1-3 PY32F003x6 series SOP16/MSOP10 product features and peripheral counts

Peripherals		PY32F003W18S6	PY32F003W16S6	PY32F003W16S6-E	PY32F003A18N6
Flash (Kbytes)		64	32	32	64
SRAM (Kbytes)		8	4	4	8
Timers	Advanced	1 (16-bit)			
	General pupose	4 (16-bit)			
	low power	1			
	SysTick	1			
	Watchdog	2			
Comm. interfaces	SPI	1			
	I^2C	1			
	USART	2			
DMA		3ch			
RTC		Yes			
GPIOs		14			8
12-bit ADC (external + internal)		10+2			5+2
Comparators		2			
Max. CPU frequency		32 MHz			24MHz
Operating Voltage		1.7 ~ 5.5 V			
Operating Temperature		-40 ~ 85 ℃			
Package		SOP16			MSOP10

Table 1-4 PY32F003x6 series SOP8/DFN8 product features and peripheral counts

Peripherals		PY32F003L18S6	PY32F003L16S6	PY32F003L28S6	PY32F003L28D6	PY32F003L26D6	PY32F003L24D6
Flash (Kbytes)		64	32	64	64	32	16
SRAM (Kbytes)		8	4	8	8	4	2
Timers	Advanced	1 (16-bit)					
	General pupose	4 (16-bit)					
	low power	1					
	SysTick	1					
	Watchdog	2					
Comm. interfaces	SPI	1					
	I^2C	1					
	USART	1					
DMA		3ch					
RTC		Yes					
GPIOs		7					
12-bit ADC (external + internal)		4+2					
Comparators		1			2		
Max. CPU frequency		24 MHz					
Operating Voltage		1.7 ~ 5.5 V					
Operating Temperature		-40 ~ 85 ℃					
Package		SOP8			DFN8(3*2)		

1-5 PY32F003x7 series QFN20/TSSOP20 product features and peripheral counts

Peripherals		PY32F003F18 U7-E	PY32F003F16 U7	PY32F003F14 U7	PY32F003F18 P7	PY32F003F16 P7	PY32F003F14 P7	PY32F003F26 P7	PY32F003F68 P7-E
Flash (Kbytes)		64	32	16	64	32	16	32	64
SRAM (Kbytes)		8	4	2	8	4	2	4	8
Timers	Advanced	1 (16-bit)							
	General pupose	4 (16-bit)							
	low power	1							
	SysTick	1							
	Watchdog	2							
Comm. interfaces	SPI	2							
	I^2C	1							
	USART	2							
DMA		3ch							
RTC		Yes							
GPIOs		18			18			18	18
12-bit ADC (external + internal)		8+2			8+2			9+2	10+2
Comparators		2							
Max. CPU frequency		32 MHz							
Operating Voltage		2.0 ~ 5.5 V							
Operating Temperature		-40 ~ 105 °C							
Package		QFN20			TSSOP20				

1-6 PY32F003x7 series SOP16 product features and peripheral counts

Peripherals		**PY32F003W18S7**
Flash (Kbytes)		64
SRAM (Kbytes)		8
Timers	Advanced	1 (16-bit)
	General pupose	4 (16-bit)
	low power	1
	SysTick	1
	Watchdog	2
Comm. interfaces	SPI	1
	I^2C	1
	USART	2
DMA		3ch
RTC		Yes
GPIOs		14
12-bit ADC (external + internal)		10+2
Comparators		2
Max. CPU frequency		32 MHz
Operating Voltage		2.0 ~ 5.5 V
Operating Temp.		-40 ~ 105 °C
Package		SOP16

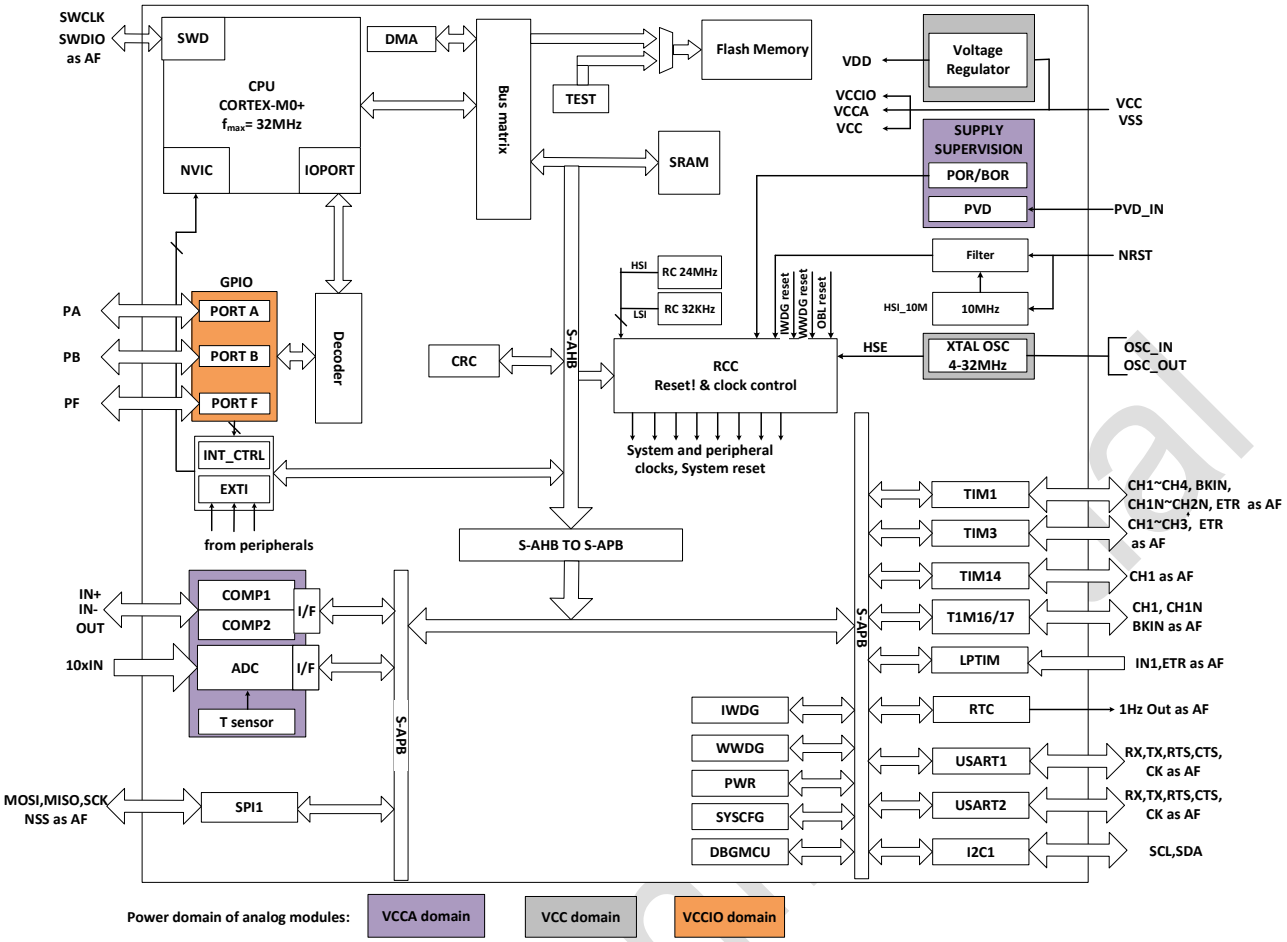


Figure 1-1 Functional Module

2. Functional overview

2.1. Arm®Cortex®-M0+ core

Arm ® The Cortex ® - M0+ is an entry-level 32-bit Arm Cortex processor designed for a wide range of embedded applications. It provides developers with significant benefits, including:

- Simple structure, easy to learn and program
- Ultra-low power consumption, energy-saving operation
- Reduced code density and more

Cortex-M0+ processor is a 32-bit core optimized for area and power consumption and is a 2-stage pipeline Von Neumann architecture. The processor offers high-end processing hardware, including single-cycle multipliers, through a streamlined but powerful instruction set and an extensively optimized design. Moreover, it delivers the superior performance expected from a 32-bit architecture computer, with a higher coding density than other 8 and 16-bit microcontrollers.

The Cortex-M0+ is tightly coupled with a Nested Vectored Interrupt Controller (NVIC).

2.2. Memories

The on-chip integrated SRAM is accessed by bytes (8 bits), half-word (16bits) or word (32bits).

The on-chip integrated Flash consists of two different physical areas:

- Main flash area, which contains application and user data
- The information area has 4K bytes, and it includes the following parts:
  - Option bytes
  - UID bytes
  - System memory

The protection of Flash main memory includes the following mechanisms:

- Read protection(RDP) prevents access from outside.
- Write protection (WRP) control prevents unwanted writes (confuse by program memory pointer from PC). The minimum protection unit for write protection is 4K bytes.
- Option byte write protection, special unlocking design.

2.3. Boot mode

Through BOOT0 pin and boot configuration bit nBOOT1 (stored in Option bytes), three different boot modes can be selected, as shown in the following table:

Table 2-1Boot configuration

Boot mode configuration		Mode
nBOOT1 bit	BOOT0 pin	
X	0	Select Main flash as the boot area
1	1	Select System memory as the boot area

Boot mode configuration		Mode
nBOOT1 bit	BOOT0 pin	
0	1	Select SRAM as the boot area

The Boot loader program is stored in the System memory and used to download the Flash program through the USART interface.

2.4. Clock System

After the CPU starts, the default system clock frequency is HSI 8 MHz, and the system clock frequency and system clock source can be reconfigured after the program runs. The high frequency clocks that can be selected are:

- A 4 /8/16/ 22.12/ 24 MHz configurable internal high precision HSI clock.
- A 32.768 KHz configurable internal LSI clock.
- 4 ~ 32 MHz HSE clock can enable the CSS function to detect HSE. If CSS fails, the hardware will automatically convert the system clock to HSI, and software configures the HSI frequency. Simultaneously, CPU NMI interrupt is generated.

The AHB clock can be divided based on the system clock, and the APB clock can be divided based on the AHB clock. AHB and APB clock frequencies up to 32 MHz.

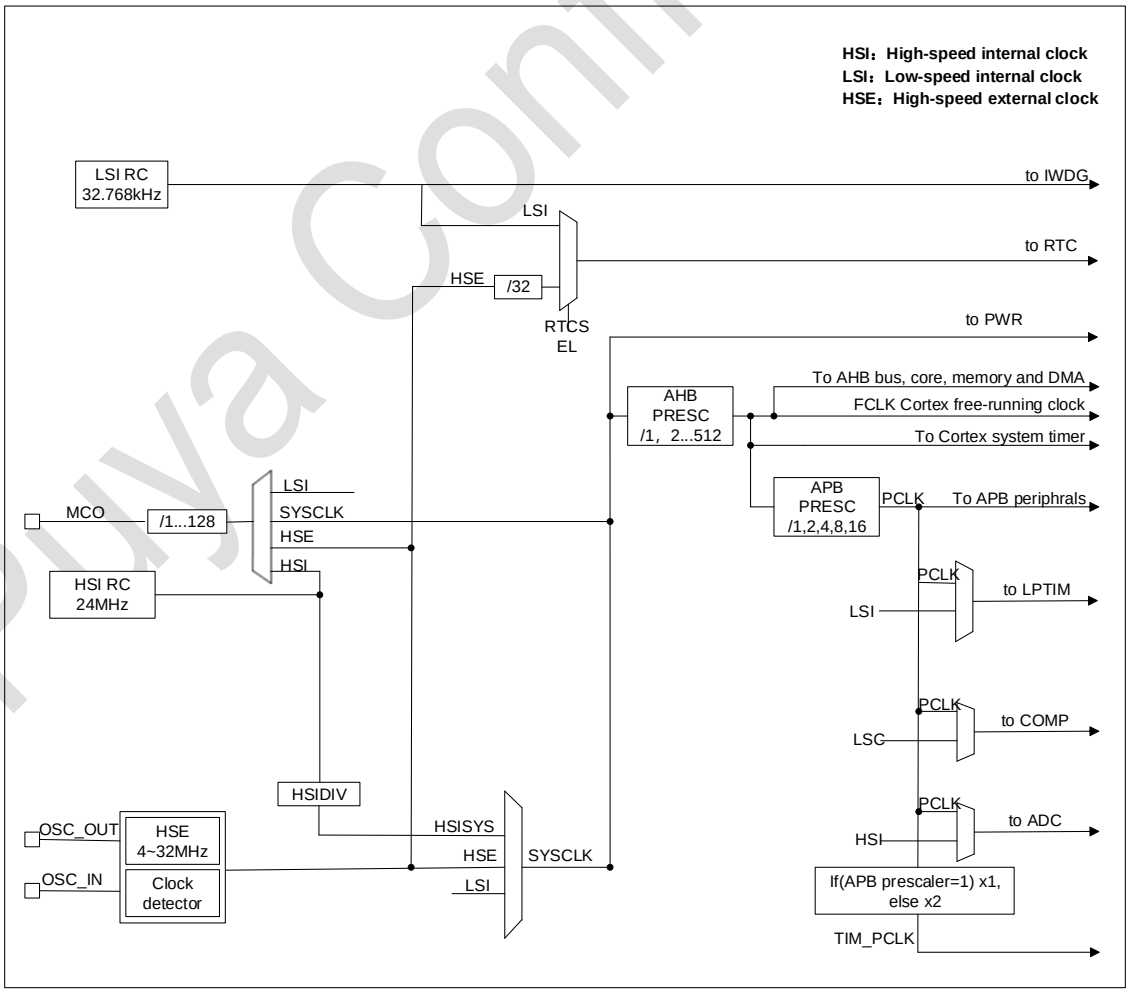


Figure 2-1 System Clock Structure Diagram

2.5. Power management

2.5.1. Power block diagram

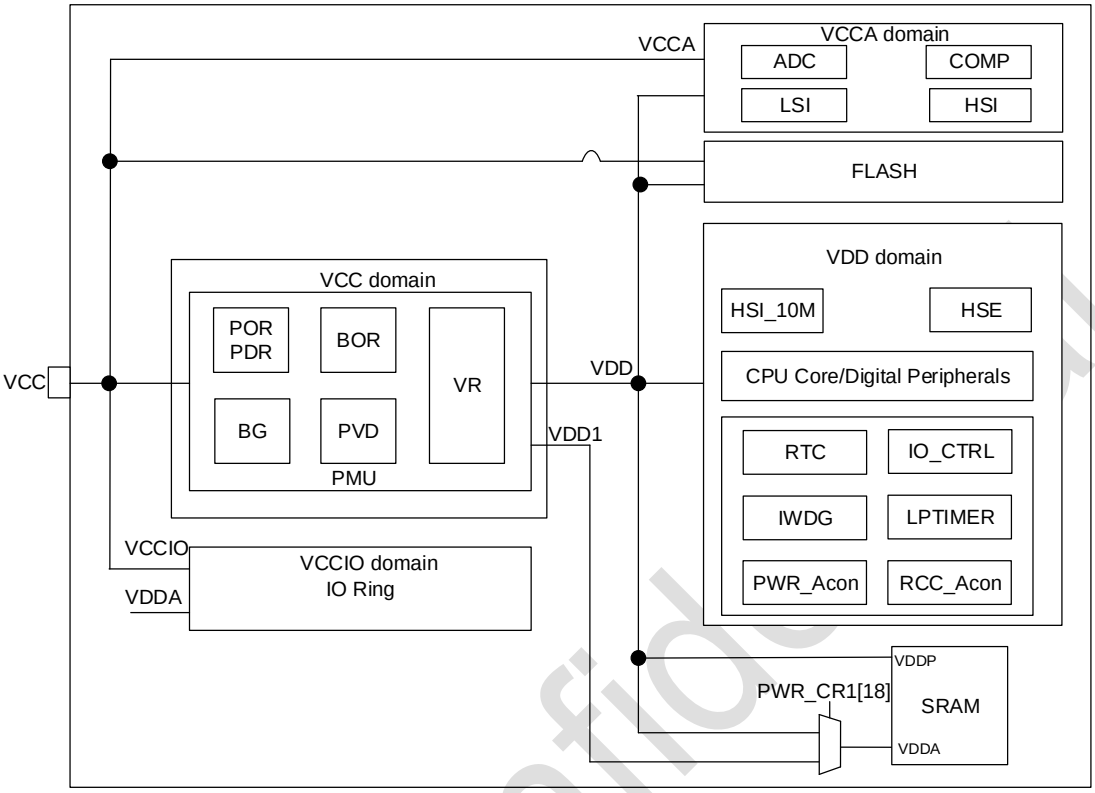


Figure 2-2 Power Block Diagram

Table 2-2 Power Block Diagram

NO.	Power supply	Condition	Power value	Describe
1	V_{CC}	x6 version	1.7 V ~ 5.5 V	The chip is supplied with power through the power pins, and its power supply module is part of the analogue circuit.
		x7 version	2.0 V ~ 5.5 V	
2	V_{CCA}	x6 version	1.7 V ~ 5.5 V	Power to most analogue modules from V_{CC} PAD (a separate power supply PAD can also be designed).
		x7 version	2.0 V ~ 5.5 V	
3	V_{CCIO}	x6 version	1.7 V ~ 5.5 V	Power supply to IO, from V_{CC} PAD
		x7 version	2.0 V ~ 5.5 V	
4	V_{DD}		1.2 V/1.0 V ± 10 %	VR supplies power to the main logic circuits and SRAM inside the chip. When the MR is powered, it outputs 1.2 V. According to the software configuration, entering the stop mode can be powered by MR or LPR, and the LPR output is determined to be 1.2 V or 1.0 V.

2.5.2. Power monitoring

2.5.2.1. Power on reset (POR/PDR)

The Power on reset (POR)/Power down reset (PDR) module is designed to provide power-on and power-off reset for the chip. The module keeps working in all modes.

2.5.2.2. Brown-out reset (BOR)

In addition to POR/ PDR, BOR (brown-out reset) is also implemented. BOR can only be enabled and disabled through the option byte.

When the BOR is turned on, the BOR threshold can be selected by the Option byte, and both the rising and falling detection points can be configured individually.

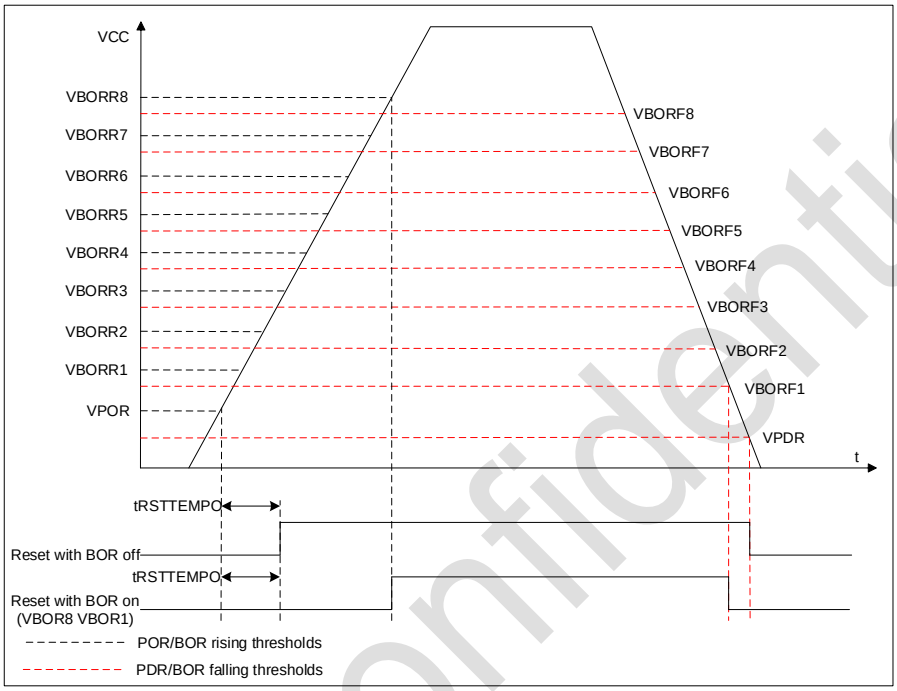


Figure 2-3 POR/PDR/BOR threshold

2.5.2.3. Voltage detection (PVD)

Programmable Voltage Detector (PVD) module can be used to detect the V_{CC} power supply (it can also detect the voltage of the PB7 pin), and the detection point can be configured through the register. When V_{CC} is higher or lower than the detection point of PVD, a corresponding reset flag is generated. This event is internally connected to line 16 of EXTI , depending on the rising/falling edge configuration of EXTI line 16. When V_{CC} rises above the PVD detection point, or V_{CC} falls below the PVD detection point , an interrupt is generated. In the service program, users can perform urgent shutdown tasks.

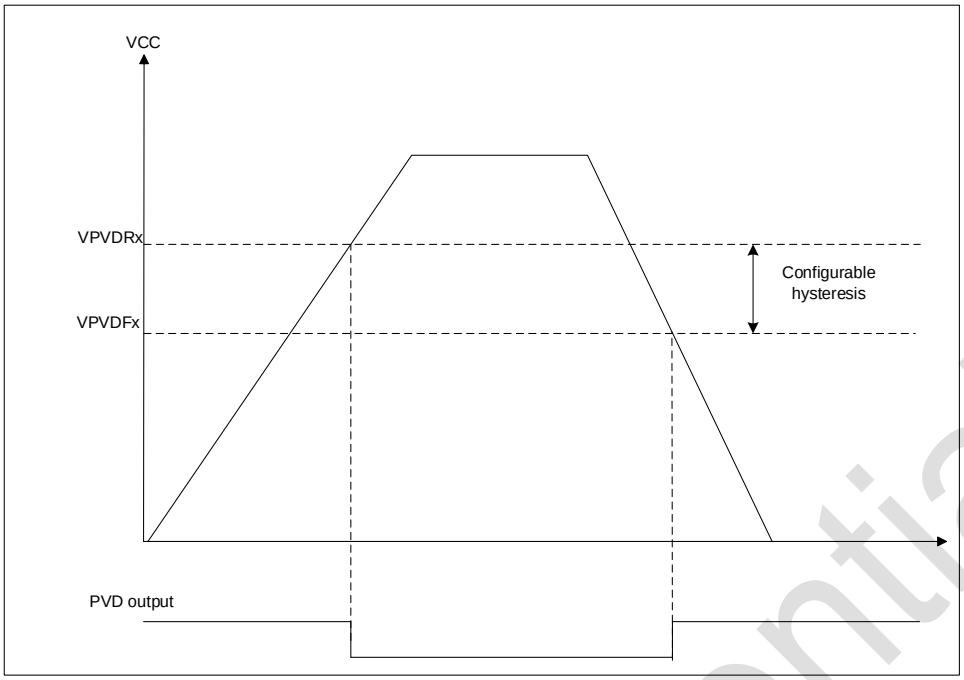


Figure 2-4 PVD Threshold

2.5.3. Voltage regulator

The chip designs two voltage regulators:

- MR (Main regulator) keeps working when the chip is in normal operating state.
- LPR (Low power regulator) provides a lower power consumption option in stop mode.

2.5.4. Low power mode

In addition to the normal operating mode, the chip has 2 low-power modes:

- **Sleep mode**: Peripherals can be configured to keep working when the CPU clock is off (NVIC, SysTick, etc.). It is recommended only to enable the modules that must work, and close the module after the module works.
- **Stop mode**: In this mode, the contents of SRAM and registers are maintained, HSI and HSE are turned off, and most modules of clocks in the V_{DD} domain are stopped. GPIO, PVD, COMP output, RTC and LPTIM can wake up stop mode.

2.6. Reset

Two resets are designed in the chip: power and system reset.

2.6.1. Power reset

A power reset occurs in the following situations:

- Power on reset (POR/PDR)
- Brown-out reset (BOR)

2.6.2. System reset

A system reset occurs when the following events occur:

- Reset of NRST pin
- Windowed Watchdog Reset (WWDG)
- Independent Watchdog Reset (IWDG)
- SYSRESETREQ software reset
- Option byte load reset (OBL)
- Power reset (POR/PDR , BOR)

2.7. General-purpose input and output (GPIOs)

The software configures each GPIO as output (push-pull or open-drain), input (floating, pull-up/down, analogue), peripheral multiplexing function, and locking mechanism freeze I/O port configuration function.

2.8. DMA

Direct Memory Access (DMA) provides high-speed data transfer between peripherals and memory or between memory and memory.

DMA controller has three channels, and each channel is responsible for managing memory access requests from one or more peripherals. The DMA controller includes an arbiter for handling DMA requests for each DMA request's priority..

DMA supports circular buffer management, eliminating the need for user code to intervene when the controller reaches the end of the buffer.

Each channel is directly connected to a dedicated hardware DMA request, and each channel also supports software triggering. These functions are configured through software.

DMA is available for peripherals: SPI, I^2C, USART, all TIMx timers (except TIM14 and LPTIM) and ADC.

2.9. Interrupt

The PY32F003 handles exceptions through the Cortex-M0+ processor's embedded Vectored Interrupt Controller (NVIC) and an Extended Interrupt/Event Controller (EXTI).

2.9.1. Interrupt controller NVIC

NVIC is a tightly coupled IP inside the Cortex-M0+ processor. The NVIC can handle NMI (Non-Maskable Interrupts) and maskable external interrupts from outside the processor and Cortex-M0+ internal exceptions. NVIC provides flexible priority management.

The tight coupling of the processor core to the NVIC greatly reduces the delay between an interrupt event and the initiation of the corresponding interrupt service routine (ISR). The ISR vectors are listed in a vector table, stored at a base address of the NVIC. The vector table base address determines the vector address of the ISR to execute, and the ISR is used as the offset composed of serial numbers.

If a high-priority interrupt event occurs and a low-priority interrupt event is just waiting to be serviced, the later-arriving high-priority interrupt event will be serviced first. Another optimization is called tail-chaining. When returning from a high-priority ISR and then starting a pending low-priority ISR, unnecessary pushes and pops of processor contexts will be skipped. This reduces latency and improves power efficiency.

NVIC features:

- Low latency interrupt handling
- Level 4 Interrupt Priority
- Supports one NMI interrupt
- Supports 32 maskable external interrupts
- Supports 10 Cortex-M0+ exceptions
- High-priority interrupts can interrupt low-priority interrupt responses
- Support tail-chaining optimization
- Hardware Interrupt Vector Retrieval

2.9.2. Extended interrupt/event controller (EXTI)

EXTI adds flexibility to handle physical wire events and generates wake-up events when the processor wakes up from stop mode.

The EXTI controller has multiple channels, including a maximum of 16 GPIOs, 1 PVD output, 2 COMP outputs, RTC and LPTIM wake-up signals. GPIO, PVD and COMP can be configured to be triggered by a rising edge, falling edge or double edge. Any GPIO signal can be configured as EXTI0 ~ 15 channel through the select signal.

Each EXTI line can be independently masked through registers.

The EXTI controller can capture pulses shorter than the internal clock period.

Registers in the EXTI controller latch each event. Even in stop mode, after the processor wakes up from stop mode, it can identify the wake-up source or identify the GPIO and event that caused the interrupt.

2.10. Analog to digital converter (ADC)

The chip has a 12-bit SAR ADC. The module has up to 12 channels to be measured, including 10 external channels and 2 internal channels.

The conversion mode of each channel can be set to single, continuous, sweep, discontinuous mode. Conversion results are stored in left or right-aligned 16-bit data registers.

An analogue watchdog allows the application to detect if the input voltage exceeds a user-defined high or low threshold.

The ADC has been implemented to operate at a low frequency, resulting in lower power consumption.

At the end of sampling, conversion, and continuous conversion, an interrupt request is generated when the conversion voltage exceeds the threshold when simulating the watchdog.

2.11. Comparators (COMP)

- Each comparator has configurable positive or negative inputs for flexible voltage selection
  - Multiple I/O pins
  - Power supply V_{CC}
  - The output of the temperature sensor
  - Internal reference voltage and 3-part values supplied by divider (1/4, 1/2, 3/4)
- The hysteresis function is configurable
- Programmable speed and power consumption
- The output can be connected to the input of I/O or timer as a trigger
  - OCREF_CLR event (current control of cycle by cycle)
  - Brakes for fast PWM shutdown

Each COMP has interrupt generation capability to act as a wake-up of the chip from low-power modes (sleep and stop modes) (via EXTI)

2.12. Timer

The characteristics of different timers of PY32F003 are shown in the following table:

Table 2-3 Timer Features

Types	Timer	Bit Width	Counting Direction	Prescaler	DMA	Capture /compare channel	Complemen-tary output
Ad-vanced	TIM1	16-bit	superior, Down, center aligned	1 ~ 65536	support	4	3
General purpose	TIM3	16-bit	superior, Down, center aligned	1 ~ 65536	support	4	-
	TIM14	16-bit	superior	1 ~ 65536	-	1	-
	TIM16, TIM17	16-bit	superior	1 ~ 65536	support	1	1

2.12.1. Advanced timer

The advanced timer (TIM1) consists of a 16-bit auto-reload counter driven by a 16-bit programmable prescaler. It can be used in various scenarios, including pulse length measurement of input signals

(input capture) or generating output waveforms (output compare, output PWM, complementary PWM with dead-time insertion).

TIM1 includes 4 independent channels:

- Input capture
- Output comparison
- PWM generation (edge or center-aligned mode)
- Single pulse mode output

If TIM1 is configured as a standard 16-bit timer, it has the same characteristics as the TIMx timer. Full modulation capability (0-100%) if configured as a 16-bit PWM generator.

In the MCU debug mode, TIM1 can freeze counting.

The timer feature with the same architecture is shared so that the TIM1 can work with other timers for synchronization or event chaining through the timer chaining function.

TIM1 supports the DMA function.

2.12.2. General-purpose timer

2.12.2.1. TIM3

The general-purpose timer TIM3 consists of a 16-bit auto-reload counter driven by a 16-bit programmable prescaler. It has 4 independent channels, each for input capture/output compare, PWM or single pulse mode output.

TIM3 can work with TIM1 through the timer link function.

TIM3 supports the DMA function.

The TIM3 can process quadrature (incremental) encoder signals and digital outputs from 1 to 3 Hall Effect Sensors.

In the MCU debug mode, the TIM 3 can freeze counting.

2.12.2.2. TIM14

The general-purpose timer TIM14 consists of a 16-bit auto-reload counter driven by a 16-bit programmable prescaler.

TIM14 has one independent channel for input capture/output compare, PWM or single pulse mode output.

In the MCU debug mode, the TIM14 can freeze counting.

2.12.2.3. TIM16/TIM17

The general-purpose timer TIM16 and TIM17 consists of a 16-bit auto-reload counter driven by a 16-bit programmable prescaler.

TIM16/TIM17 have 1 independent channel for input capture/output compare, PWM or single pulse mode output.

TIM16/TIM17 have one independent channel for input capture/output compare, PWM or single pulse mode output.

TIM16/TIM17 have complementary outputs with dead time.

TIM16/TIM17 supports the DMA function.

In the MCU debug mode, TIM 16/TIM17 can freeze counting.

2.12.3. Low power timer (LPTIM)

LPTIM is a 16 -bit up counter with a 3-bit prescaler and only support a single count.

LPTIM can be configured as a stop mode wakeup source.

In the MCU debug mode, LPTIM can freeze the count value.

2.12.4. IWDG

Independent watchdog (IWDG) is integrated in the chip, and this module has the characteristics of high-security level, accurate timing and flexible use. IWDG finds and resolves functional confusion due to software failure and triggers a system reset when the counter reaches the specified timeout value.

The IWDG is clocked by LSI, so even if the main clock fails, it can keep working.

IWDG is the best suited for applications that require the watchdog as a standalone process outside of the main application and do not have high timing accuracy constraints.

Controlling of option byte can enable IWDG hardware mode.

IWDG is the wake-up source of stop mode, which wakes up stop mode by reset.

In the MCU debug mode, IWDG can freeze the count value.

2.12.5. WWDG

The system window watchdog is based on a 7-bit down counter and can be set to free-run. It acts as a watchdog to reset the system when a failure shows. The count clock is the APB clock (PCLK). It has early warning interrupt capability, and the counter can be freeze in the MCU debug mode.

2.12.6. SysTick timer

SysTick counters are specifically for real-time operating systems (RTOS) also can use as standard down counters.

SysTick Features:

- 24-bit count down
- Self-loading capability
- An interrupt can be generated when the counter reaches 0 (maskable)

2.13. Real time clock (RTC)

The real-time clock is an independent timer. It has a set of continuous counting counters, which can provide a clock calendar function under the corresponding software configuration. Modifying the value of the counter can reset the current time and date of the system.

RTC is a 32-bit programmable counter with a prescale factor of up to 2^{20} bits.

The RTC counter clock source can be LSI and the stop wake-up source.

RTC can generate alarm interrupt, second interrupt and overflow interrupt (maskable).

RTC supports clock calibration.

In the MCU debug mode, RTC can freeze counting.

2.14. I2C interface

I^2C (inter-integrated circuit) bus interface connects the microcontroller and the serial I^2C bus. It provides multi-master capability and controls all I^2C bus specific sequences, protocols, arbitration and timing. Standard (Sm) and fast (Fm) are supported.

I^2C Features:

- Slave and master mode
- Multi-host function: can be master or slave
- Support different communication speeds
  - Standard Mode (Sm): Up to 100 kHz
  - Fast Mode (Fm): up to 400 kHz
- As master
  - Generate Clock
  - Generation of Start and Stop
- As slave
  - Programmable I2C address detection
  - Discovery of the Stop bit
- 7-bit addressing mode
- General call
- Status flag
  - Transmit/receive mode flags
  - Byte transfer complete flag
  - I^2C busy flag bit
- Error flag
  - Master a rbitration loss
  - ACK failure after address/data transfer
  - Start/Stop error
  - Overrun/Underrun (clock stretching function disable)

- Optional Clock Stretching
- Single-byte buffer with DMA capability
- Software reset
- Analogue noise filter function

2.15. Universal synchronous asynchronous recevicer/ transmitter (USART)

PY32F003 contains 2 USARTs with precisely the same functions.

The Universal Synchronous Asynchronous Transceiver (USART) provides a flexible method for full-duplex data exchange with external devices using the industry-standard NRZ asynchronous serial data format. The USART utilizes a fractional baudrate generator to provide a wide range of baudrate options.

It supports simultaneous one-way communication and half-duplex single-wire communication, and it also allows multi-processor communication.

Automatic baudrate detection is supported.

High-speed data communication can be achieved by using the DMA method of the multi-buffer configuration.

USART features:

- Full-duplex asynchronous communication
- NRZ standard format
- Configurable 16 times or 8 times oversampling for increased flexibility in speed and clock tolerance
- Programmable baudrate shared by transmit and receive, up to 4.5 Mbit/s
- Automatic baudrate detection
- Programmable data length of 8 or 9 bits
- Configurable stop bits (1 bit or 2 bits)
- Synchronous mode and clock output function for synchronous communication
- Single-wire half-duplex communication
- Independent transmit and receive enable bits
- Hardware flow control
- Receive/transmit bytes by DMA buffer
- Detection flag
  - Receive full buffer
  - Send empty buffer
  - End of transmission
- Parity Control
  - Send check digit
  - Check the received data

- Flagged interrupt sources
  - CTS change
  - Send empty register
  - Send completed
  - Receive full data register
  - Bus idle detected
  - Overflow error
  - Frame error
  - Noise operation
  - Error detection
- Multiprocessor communication
  - If the address does not match, enter silent mode
- Wake-up from silent mode: by idle detection and address flag detection

2.16. Serial peripheral interface (SPI)

PY32F003 contains one SPI.

Serial Peripheral Interface (SPI) allows the chip to communicate with external devices in half-duplex, full-duplex, and simplex synchronous serial communication. This interface can be configured in master mode and provides the communication clock (SCK) for external slave devices. The interface can also work in a multi-master configuration.

The SPI features are as follows:

- Master or slave mode
- 3 -wire full-duplex simultaneous transmission
- 2-wire half-duplex synchronous transmission (with bidirectional data line)
- 2-wire simplex synchronous transmission (no bidirectional data line)
- 8-bit or 16-bit transmission frame selection
- Support multi-master mode
- 8 master mode baudrate prescaler factors (max f_{PCLK}/ 4)
- Slave mode frequency (max f_{PCLK}/4)
- Both master and slave modes can be managed by software or hardware NSS: dynamic change of master/slave operating mode
- Programmable clock polarity and phase
- Programmable data order, MSB first or LSB first
- Dedicated transmit and receive flags that can trigger interrupts
- SPI bus busy status flag
- Motorola mode
- Interrupt-causing master mode faults, overloads
- Two 32-bit Rx and Tx FIFOs with DMA capability

2.17. SWD

The ARM SWD interface allows serial debugging tools to be connected to the PY32F003.

3. Pin configuration

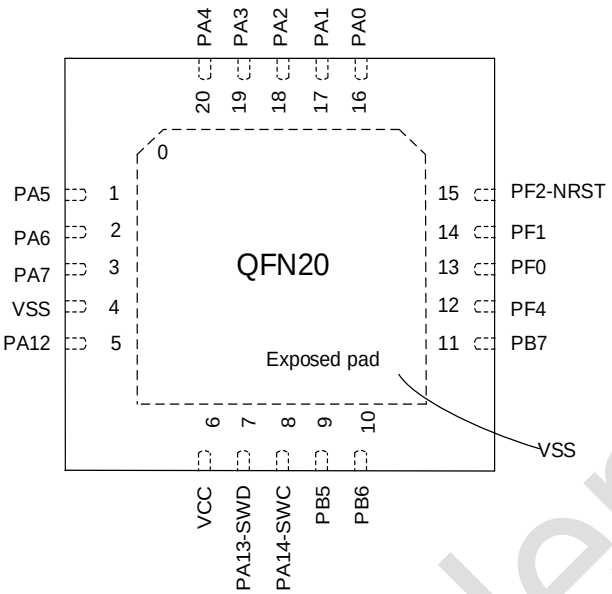


Figure 3-1 QFN20 Pinout1 PY32F003F1xUx / PY32F003F1xUx-E

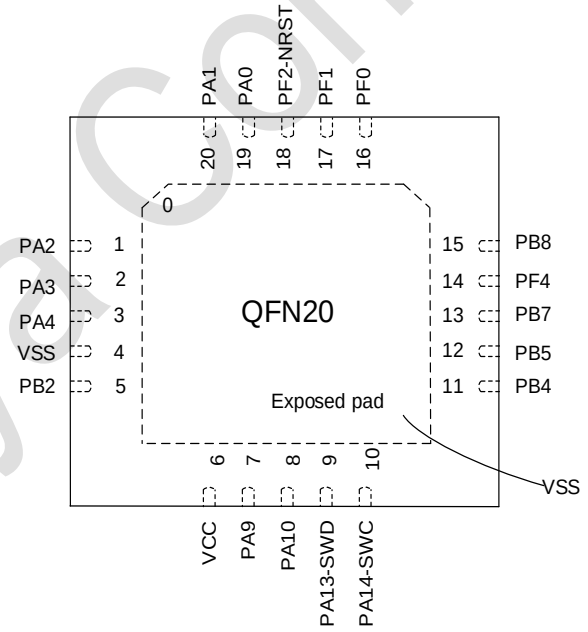


Figure 3-2 QFN20 Pinout2 PY32F003F2xUx

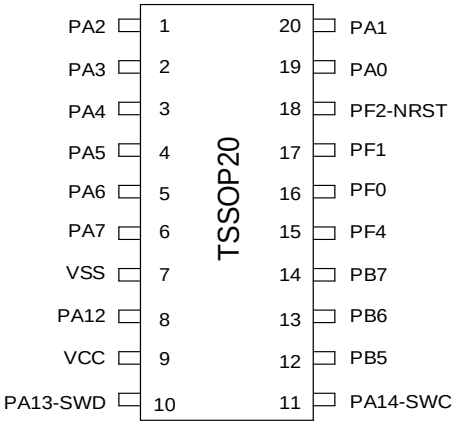


Figure 3-3 TSSOP20 Pinout1 PY32F003F1xPx / PY32F003F1xPx-E

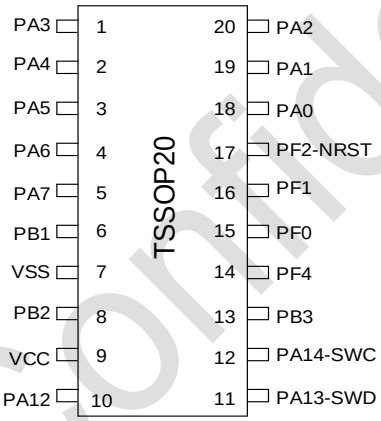


Figure 3-4 TSSOP20 Pinout2 PY32F003F2xPx

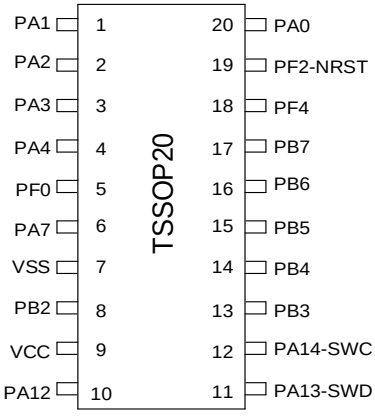


Figure 3-5 TSSOP20 Pinout3 PY32F003F3xPx

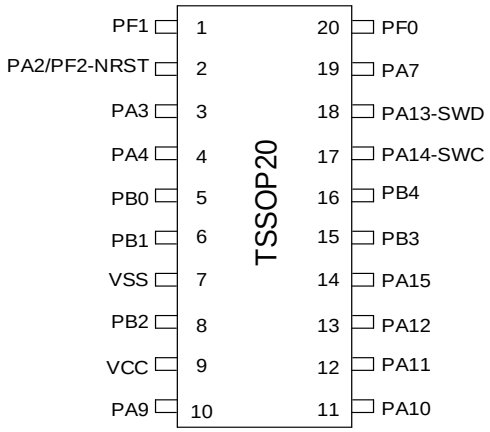


Figure 3-6 TSSOP20 Pinout4 PY32F003F4xPx

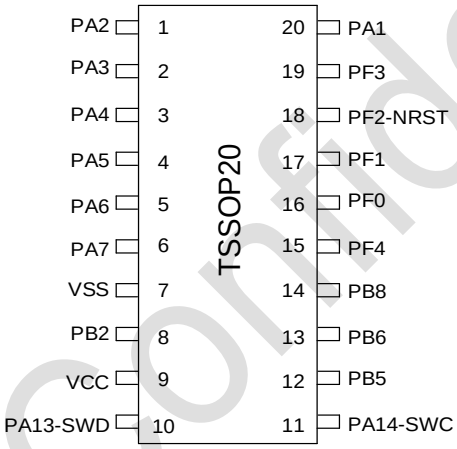


Figure 3-7 TSSOP20 Pinout5 PY32F003F5xPx

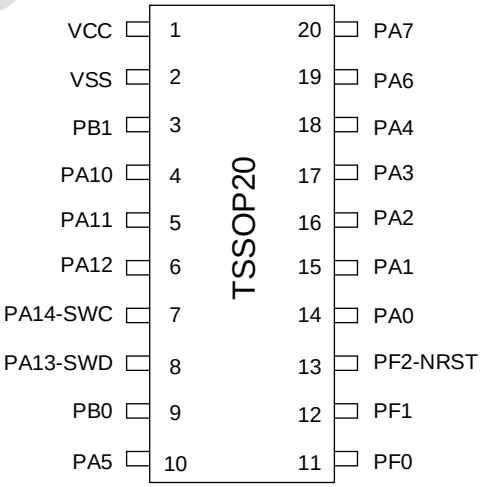


Figure 3-8 TSSOP20 Pinout6 PY32F003F6xPx / PY32F003F6xPx-E

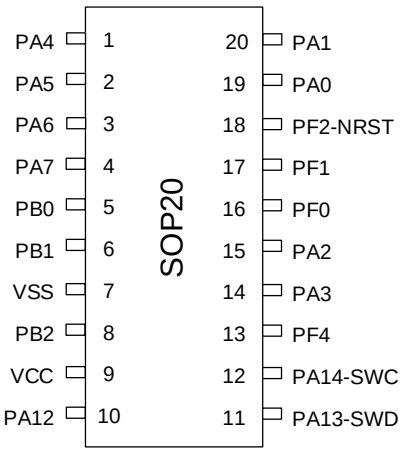


Figure 3-9 SOP20 Pinout1 PY32F003F1xSx

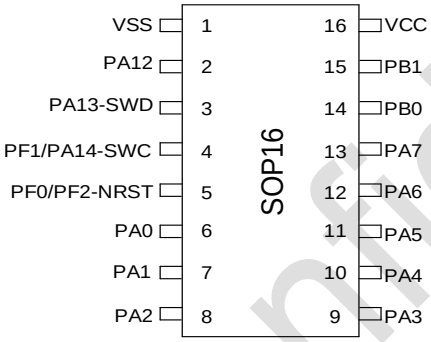


Figure 3-10 SOP16 Pinout1 PY32F003W1xSx / PY32F003W1xSx-E

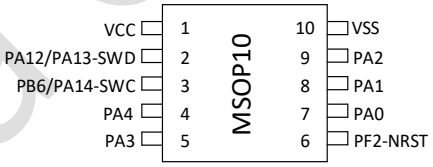


Figure 3-11 MSOP10 PY32F003A1xNx

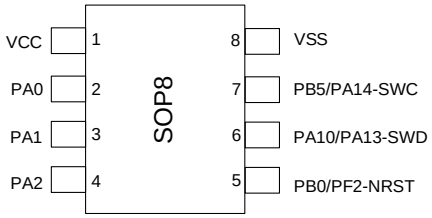


Figure 3-12 SOP8 PY32F003L1xSx

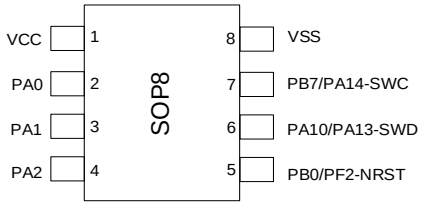


Figure 3-13 SOP8 PY32F003L2xSx

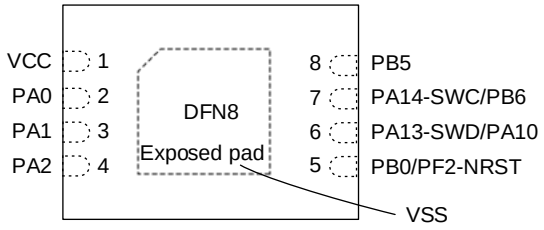


Figure 3-14 DFN8(3*2) PY32F003L2xDx

Table 3-1 Pin definition terminology and symbols

Types		Symbol	Definition
Port type		S	Supply pin
		G	Ground p in
		I/O	Input/output pin
		NC	Undefined
Port structure		COM	5V port, support analogue input and output function
		RST	Reset port, with internal weak pull-up resistor, does not support analog input and output function
Notes		-	Unless other specified, all ports are used as floating inputs between and after reset
Port function	Multiplexing function	-	Function selected by GPIOx_AFR register
	Additional function	-	Directly selected or enabled through peripheral registers

Table 3-2 QFN20/TSSOP20/SOP20 pin definition

Packages									Reset	Port type	Port structure	Notes	Functions	
QFN20 F1	QFN20 F2	TSSOP20 F1	TSSOP20 F2	TSSOP20 F3	TSSOP20 F4	TSSOP20 F5	TSSOP20 F6	SOP20 F1					Multiplexing	Additional
13	16	16	15	5	20	16	11	16	PF0-OSC_IN	I/O	COM		USART2_RX	OSC_IN
													TIM14_CH1	
													USART1_RX	
													USART2_TX	
													I^2C_SDA	
14	17	17	16	-	1	17	12	17	PF1-OSC_OUT	I/O	COM		USART2_TX	OSC_OUT
													USART1_TX	
													USART2_RX	
													I^2C_SCL	
													SPI1_NSS	
													TIM14_CH1	
15	18	18	17	19	2	18	13	18	PF2-NRST	I/O	RST	(1)	MCO	NRST
													USART2_RX	
-	-	-	-	-	-	19	-	-	PF3	I/O	COM		USART1_TX	COMP2_INP
													USART2_TX	
													RTC_OUT	
													SPI1_NSS	
													TIM3_CH3	
16	19	19	18	20	-	-	14	19	PA0	I/O	COM		USART1_CTS	ADC_IN0 COMP1_INM
													USART2_CTS	
													COMP1_OUT	
													TIM1_CH3	
													TIM1_CH1N	

Packages									Reset	Port type	Port structure	Notes	Functions	
QFN20 F1	QFN20 F2	TSSOP20 F1	TSSOP20 F2	TSSOP20 F3	TSSOP20 F4	TSSOP20 F5	TSSOP20 F6	SOP20 F1					Multiplexing	Additional
													SPI1_MISO	
													USART2_TX	
													IR_OUT	
17	20	20	19	1	-	20	15	20	PA1	I/O	COM		SPI1_SCK	ADC_IN1 COMP1_INP
													USART1_RTS	
													USART2_RTS	
													EVENTOUT	
													SPI1_MOSI	
													USART2_RX	
													TIM1_CH4	
													TIM1_CH2N	
													MCO	
18	1	1	20	2	2	1	16	15	PA2	I/O	COM		SPI1_MOSI	ADC_IN2 COMP2_INM
													USART1_TX	
													USART2_TX	
													COMP2_OUT	
													SPI1_SCK	
													TIM3_CH1	
													I^2C_SDA	
19	2	2	1	3	3	2	17	14	PA3	I/O	COM		USART1_RX	ADC_IN3 COMP2_INP
													USART2_RX	
													EVENTOUT	
													SPI1_MOSI	
													TIM1_CH1	
													I^2C_SCL	

Packages									Reset	Port type	Port structure	Notes	Functions	
QFN20 F1	QFN20 F2	TSSOP20 F1	TSSOP20 F2	TSSOP20 F3	TSSOP20 F4	TSSOP20 F5	TSSOP20 F6	SOP20 F1					Multiplexing	Additional
20	3	3	2	4	4	3	18	1	PA4	I/O	COM		SPI1_NSS USART1_CK TIM14_CH1 USART2_CK ENENTOUT RTC_OUT TIM3_CH3 USART2_TX	ADC_IN4
1	-	4	3	-	-	4	10	2	PA5	I/O	COM		SPI1_SCK LPTIM_ETR EVENTOUT TIM3_CH2 USART2_RX MCO	ADC_IN5
2	-	5	4	-	-	5	19	3	PA6	I/O	COM		SPI1_MISO TIM3_CH1 TIM1_BKIN TIM16_CH1 COMP1_OUT USART1_CK RTC_OUT	ADC_IN6
3	-	6	5	6	19	6	20	4	PA7	I/O	COM		SPI1_MOSI TIM3_CH2 TIM1_CH1N TIM14_CH1	ADC_IN7

Packages									Reset	Port type	Port structure	Notes	Functions	
QFN20 F1	QFN20 F2	TSSOP20 F1	TSSOP20 F2	TSSOP20 F3	TSSOP20 F4	TSSOP20 F5	TSSOP20 F6	SOP20 F1					Multiplexing	Additional
													TIM17_CH1	
													EVENTOUT	
													COMP2_OUT	
													USART1_TX	
													USART2_TX	
													I^2C_SDA	
													SPI1_MISO	
-	-	-	-	-	5	-	9	5	PB0	I/O	COM		SPI1_NSS	ADC_IN8
													TIM3_CH3	
													TIM1_CH2N	
													EVENTOUT	
													COMP1_OUT	
-	-	-	6	-	6	-	3	6	PB1	I/O	COM		TIM14_CH1	ADC_IN9 COMP1_INM
													TIM3_CH4	
													TIM1_CH3N	
													EVENTOUT	
4	4	7	7	7	7	-	2	7	V_{SS}	S			Ground	
-	5	-	8	8	8	8	-	8	PB2	I/O	COM		USART1_RX	COMP1_INP
													USART2_RX	
6	6	9	9	9	9	9	1	9	V_{CC}	S			Digital power supply	
-	-	-	-	-	-	-	-	-	PA8	I/O	COM		USART1_CK	-
													TIM1_CH1	
													USART2_CK	
													MCO	
													EVENTOUT	

Packages									Reset	Port type	Port structure	Notes	Functions	
QFN20 F1	QFN20 F2	TSSOP20 F1	TSSOP20 F2	TSSOP20 F3	TSSOP20 F4	TSSOP20 F5	TSSOP20 F6	SOP20 F1					Multiplexing	Additional
													USART1_RX	
													USART2_RX	
													SPI1_MOSI	
													I^2C_SCL	
-	7	-	-	-	10	-	-	-	PA9	I/O	COM		USART1_TX	OSC32OUT
													TIM1_CH2	
													MCO	
													I^2C_SCL	
													EVENTOUT	
													I^2C_SDA	
													TIM1_BK	
													SPI1_SCK	
													USART1_RX	
-	8	-	-	-	11	-	4	-	PA10	I/O	COM		USART1_RX	OS32IN
													TIM1_CH3	
													TIM17_BKIN	
													USART2_RX	
													I^2C_SDA	
													EVENTOUT	
													I^2C_SCL	
													SPI1_NSS	
													USART1_TX	
													IR_OUT	
-	-	-	-	-	12	-	5	-	PA11	I/O	COM		SPI1_MISO	-
													USART1_CTS	

Packages									Reset	Port type	Port structure	Notes	Functions	
QFN20 F1	QFN20 F2	TSSOP20 F1	TSSOP20 F2	TSSOP20 F3	TSSOP20 F4	TSSOP20 F5	TSSOP20 F6	SOP20 F1					Multiplexing	Additional
													TIM1_CH4	
													EVENTOUT	
													USART2_CTS	
													I^2C_SCL	
													COMP1_OUT	
5	-	8	10	10	13	-	6	10	PA12	I/O	COM		SPI1_MOSI	-
													USART1_RTS	
													TIM1_ETR	
													USART2_RTS	
													EVENTOUT	
													I^2C_SDA	
													COMP2_OUT	
7	9	10	11	11	18	10	8	11	PA13 (SWDIO)	I/O	COM	(2)	SWDIO	-
													IR_OUT	
													EVENTOUT	
													SPI1_MISO	
													TIM1_CH2	
													USART1_RX	
													MCO	
8	10	11	12	12	17	11	7	12	PA14 (SWCLK)	I/O	COM	(2)	SWCLK	-
													USART1_TX	
													USART2_TX	
													EVENTOUT	
													MCO	
-	-	-	-	-	14	-	-	-	PA15	I/O	COM		SPI1_NSS	-

Packages									Reset	Port type	Port structure	Notes	Functions	
QFN20 F1	QFN20 F2	TSSOP20 F1	TSSOP20 F2	TSSOP20 F3	TSSOP20 F4	TSSOP20 F5	TSSOP20 F6	SOP20 F1					Multiplexing	Additional
													USART1_RX	
													USART2_RX	
													EVENTOUT	
-	-	-	13	13	15	-	-	-	PB3	I/O	COM		SPI1_SCK	COMP2_INM
													TIM1_CH2	
													USART1_RTS	
													USART2_RTS	
													EVENTOUT	
-	11	-	-	14	16	-	-	-	PB4	I/O	COM		SPI1_MISO	COMP2_INP
													TIM3_CH1	
													USART2_CTS	
													USART1_CTS	
													TIM17_BKIN	
													EVENTOUT	
9	12	12	-	15	-	12	-	-	PB5	I/O	COM		SPI1_MOSI	-
													TIM3_CH2	
													TIM16_BKIN	
													USART2_CK	
													USART1_CK	
													LPTIM_IN1	
													COMP1_OUT	
10	-	13	-	16	-	13	-	-	PB6	I/O	COM		USART1_TX	COMP2_INP
													TIM1_CH3	
													TIM16_CH1N	
													USART2_TX	

Packages									Reset	Port type	Port structure	Notes	Functions	
QFN20 F1	QFN20 F2	TSSOP20 F1	TSSOP20 F2	TSSOP20 F3	TSSOP20 F4	TSSOP20 F5	TSSOP20 F6	SOP20 F1					Multiplexing	Additional
													I^2C_SCL	
													LPTIM_ETR	
													EVENTOUT	
11	13	14	-	17	-	-	-	-	PB7	I/O	COM		USART1_RX	COMP2_INM PVD_IN
													TIM17_CH1N	
													USART2_RX	
													I^2C_SDA	
													EVENTOUT	
12	14	15	14	18	-	15	-	13	PF4-BOOT0	I/O	COM	(3)	-	BOOT0
-	15	-	-	-	-	14	-	-	PB8	I/O	COM		TIM16_CH1	COMP1_INP
													I^2C1_SCL	
													USART2_TX	
													EVENTOUT	
													USART1_TX	
													I^2C_SDA	
													TIM17_CH1	
													IR_OUT	
-	-	-	-	-	-	-	-	-	V_{SS}	S			Ground	

1. Selecting PF2 or NRST is configured through option bytes .
2. After reset, the two pins of PA13 and PA14 are configured as SWDIO and SWCLK AF function, the former internal pull-up resistor, the latter internal pull-down resistor is activated.
3. PF4 -BOOT0 is the default digital input mode, and the pull-down is enabled.

Table 3-3 SOP16/MSOP10 pin definition

Packages		Reset	Port type	Port structure	Notes	Functions	
SOP16 W1	MSOP10 P1					Multiplexing	Additional
1	10	VSS	S			Ground	
2	2	PA12	I/O	COM		SPI1_MOSI USART1_RTS TIM1_ETR USART2_RTS EVENTOUT I2C_SDA COMP2_OUT	-
3	2	PA13(SWDIO)	I/O	COM	(2)	SWDIO IR_OUT EVENTOUT SPI1_MISO TIM1_CH2 USART1_RX MCO	-
4	-	PF1-OSC_OUT- (PF1)	I/O	COM		USART2_TX USART1_TX USART2_RX I2C_SCL SPI1_NSS TIM14_CH	OSC_OUT
4	3	PA14(SWCLK)	I/O	COM	(2)	SWCLK USART1_TX USART2_TX	-

Packages		Reset	Port type	Port structure	Notes	Functions	
SOP16 W1	MSOP10 P1					Multiplexing	Additional
						EVENTOUT	
						MCO	
-	3	PB6	I/O	COM		USART1_TX	COMP2_INP
						TIM1_CH3	
						TIM16_CH1N	
						USART2_TX	
						I2C_SCL	
						LPTIM_ETR	
						EVENTOUT	
5	-	PF0-OSC_IN-（PF0）	I/O	COM		USART2_RX	OSC_IN
						TIM14_CH1	
						USART1_RX	
						USART2_TX	
						I2C_SDA	
5	6	PF2-NRST	I/O	RST	(1)	MCO	NRST
						USART2_RX	
6	7	PA0	I/O	COM		USART1_CTS	ADC_IN0 COMP1_INM
						USART2_CTS	
						COMP1_OUT	
						TIM1_CH3	
						TIM1_CH1N	
						SPI1_MISO	
						USART2_TX	
						IR_OUT	
7	8	PA1	I/O	COM		SPI1_SCK	

Packages		Reset	Port type	Port structure	Notes	Functions	
SOP16 W1	MSOP10 P1					Multiplexing	Additional
						USART1_RTS	COMP1_INP ADC_IN1
						USART2_RTS	
						EVENTOUT	
						SPI1_MOSI	
						USART2_RX	
						TIM1_CH4	
						TIM1_CH2N	
						MCO	
8	9	PA2	I/O	COM		SPI1_MOSI	COMP2_INM ADC_IN2
						USART1_TX	
						USART2_TX	
						COMP2_OUT	
						SPI1_SCK	
						TIM3_CH1	
						I2C_SDA	
9	5	PA3	I/O	COM		USART1_RX	COMP2_INP ADC_IN3
						USART2_RX	
						EVENTOUT	
						SPI1_MOSI	
						TIM1_CH1	
						I2C_SCL	
10	4	PA4	I/O	COM		SPI1_NSS	ADC_IN4
						USART1_CK	
						TIM14_CH1	
						USART2_CK	

Packages		Reset	Port type	Port structure	Notes	Functions	
SOP16 W1	MSOP10 P1					Multiplexing	Additional
						ENENTOUT	
						RTC_OUT	
						TIM3_CH3	
						USART2_TX	
11	-	PA5	I/O	COM		SPI1_SCK	ADC_IN5
						LPTIM_ETR	
						EVENTOUT	
						TIM3_CH2	
						USART2_RX	
						MCO	
12	-	PA6	I/O	COM		SPI1_MISO	ADC_IN6
						TIM3_CH1	
						TIM1_BKIN	
						TIM16_CH1	
						EVENTOUT	
						COMP1_OUT	
						USART1_CK	
						RTC_OUT	
13	-	PA7	I/O	COM		SPI1_MOSI	ADC_IN7
						TIM3_CH2	
						TIM1_CH1N	
						TIM14_CH1	
						TIM17_CH1	
						EVENTOUT	
						COMP2_OUT	

Packages		Reset	Port type	Port structure	Notes	Functions	
SOP16 W1	MSOP10 P1					Multiplexing	Additional
						USART1_TX	
						USART2_TX	
						I2C_SDA	
						SPI1_MISO	
14	-	PB0	I/O	COM		SPI1_NSS	ADC_IN8
						TIM3_CH3	
						TIM1_CH2N	
						EVENTOUT	
						COMP1_OUT	
15	-	PB1	I/O	COM		TIM14_CH1	COMP1_INM ADC_IN9
						TIM3_CH4	
						TIM1_CH3N	
						EVENTOUT	
16	1	VCC	S			Digital power supply	

1. Selecting PF2 or NRST is configured through option bytes .
2. After reset, the two pins of PA13 and PA14 are configured as SWDIO and SWCLK AF function, the former internal pull-up resistor, the latter internal pull-down resistor is activated.

Table 3-4 SOP8 pin definition

Packages		Reset	Port type	Port structure	Notes	Functions	
SOP8 L1	SOP8 L2					Multiplexing	Additional
1	1	VCC	S			Digital power supply	
2	2	PA0	I/O	COM		USART1_CTS	ADC_IN0 COMP1_INM
						COMP1_OUT	
						TIM1_CH3	
						TIM1_CH1N	
						SPI1_MISO	
						IR_OUT	
3	3	PA1	I/O	COM		SPI1_SCK	COMP1_INP ADC_IN1
						USART1_RTS	
						EVENTOUT	
						SPI1_MOSI	
						TIM1_CH4	
						TIM1_CH2N	
						MCO	
4	4	PA2	I/O	COM		SPI1_MOSI	ADC_IN2
						USART1_TX	
						SPI1_SCK	
						TIM3_CH1	
						I2C_SDA	
5	5	PF2-NRST	I/O	RST	(1)	MCO	NRST
		PB0	I/O	COM		SPI1_NSS	ADC_IN8
						TIM3_CH3	
						TIM1_CH2N	
						EVENTOUT	
						COMP1_OUT	
6	6	PA10	I/O	COM		USART1_RX	

Packages		Reset	Port type	Port structure	Notes	Functions	
SOP8 L1	SOP8 L2					Multiplexing	Additional
						TIM1_CH3	
						TIM17_BKIN	
						I2C_SDA	
						EVENTOUT	
						I2C_SCL	
						SPI1_NSS	
						USART1_TX	
						IR_OUT	
		PA13(SWDIO)	I/O	COM	(2)	SWDIO	-
						IR_OUT	
						EVENTOUT	
						SPI1_MISO	
						TIM1_CH2	
						USART1_RX	
						MCO	
7	7	PA14(SWCLK)	I/O	COM	(2)	SWCLK	-
						USART1_TX	
						EVENTOUT	
						MCO	
	-	PB5	I/O	COM_L		SPI1_MOSI	
						TIM3_CH2	
						TIM16_BKIN	
						USART1_CK	
						LPTIM_IN1	
						COMP1_OUT	
-	7	PB7	I/O	COM_L		USART1_RX	COMP2_INM PVD_IN

Packages		Reset	Port type	Port struc-ture	Notes	Functions	
SOP8 L1	SOP8 L2					Multiplexing	Additional
						TIM17_CH1N	
						USART2_RX	
						I2C_SDA	
						EVENTOUT	
8	-	VSS	S			Digital power supply	

1. Selecting PF2 or NRST is configured through option bytes .
2. After reset, the two pins of PA13 and PA14 are configured as SWDIO and SWCLK AF function, the former internal pull-up resistor, the latter internal pull-down resistor is activated.

Table 3-5 DFN8 pin definition

Packages	Reset	Port type	Port structure	Notes	Functions	
DFN8 L2					Multiplexing	Additional
1	VCC	S			Digital power supply	
2	PA0	I/O	COM		USART1_CTS	ADC_IN0 COMP1_INM
					COMP1_OUT	
					TIM1_CH3	
					TIM1_CH1N	
					SPI1_MISO	
					IR_OUT	
3	PA1	I/O	COM		SPI1_SCK	COMP1_INP ADC_IN1
					USART1_RTS	
					EVENTOUT	
					SPI1_MOSI	

Packages	Reset	Port type	Port structure	Notes	Functions	
DFN8 L2					Multiplexing	Additional
					TIM1_CH4	
					TIM1_CH2N	
					MCO	
4	PA2	I/O	COM		SPI1_MOSI	COMP2_INM ADC_IN2
					USART1_TX	
					COMP2_OUT	
					SPI1_SCK	
					TIM3_CH1	
					I2C_SDA	
5	PF2-NRST	I/O	RST	(1)	MCO	NRST
	PB0	I/O	COM		SPI1_NSS	ADC_IN8
					TIM3_CH3	
					TIM1_CH2N	
					EVENTOUT	
					COMP1_OUT	
6	PA10	I/O	COM		USART1_RX	OS32IN
					TIM1_CH3	
					TIM17_BKIN	
					I2C_SDA	
					EVENTOUT	
					I2C_SCL	
					SPI1_NSS	
					USART1_TX	
					IR_OUT	
	PA13(SWDIO)	I/O	COM	(2)	SWDIO	-
					IR_OUT	

Packages	Reset	Port type	Port structure	Notes	Functions	
DFN8 L2					Multiplexing	Additional
					EVENTOUT	
					SPI1_MISO	
					TIM1_CH2	
					USART1_RX	
					MCO	
7	PA14(SWCLK)	I/O	COM	(2)	SWCLK	-
					USART1_TX	
					EVENTOUT	
					MCO	
	PB6	I/O	COM		USART1_TX	COMP2_INP
					TIM1_CH3	
					TIM16_CH1N	
					I2C_SCL	
					LPTIM_ETR	
					EVENTOUT	
8	PB5	I/O	COM_L		SPI1_MOSI	-
					TIM3_CH2	
					TIM16_BKIN	
					USART1_CK	
					LPTIM_IN1	
					COMP1_OUT	

1. Selecting PF2 or NRST is configured through option bytes .
2. After reset, the two pins of PA13 and PA14 are configured as SWDIO and SWCLK AF function, the former internal pull-up resistor, the latter internal pull-down resistor is activated.

3.1. Port A multiplexing function mapping

Table 3-6 Port A multiplexing function mapping

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PA0	-	USART1_CTS	-	-	USART2_CTS	-	-	COMP1_OUT
	AF8	**AF9**	**AF10**	**AF11**	**AF12**	**AF13**	**AF14**	**AF15**
	-	USART2_TX	SPI1_MISO	-	-	TIM1_CH3	TIM1_CH1N	IR_OUT
PA1	**AF0**	**AF1**	**AF2**	**AF3**	**AF4**	**AF5**	**AF6**	**AF7**
	SPI1_SCK	USART1_RTS	-	-	USART2_RTS	-	-	EVENTOUT
	AF8	**AF9**	**AF10**	**AF11**	**AF12**	**AF13**	**AF14**	**AF15**
	-	USART2_RX	SPI1_MOSI	-	-	TIM1_CH4	TIM1_CH2N	MCO
PA2	**AF0**	**AF1**	**AF2**	**AF3**	**AF4**	**AF5**	**AF6**	**AF7**
	SPI1_MOSI	USART1_TX	-	-	USART2_TX	-	-	COMP2_OUT
	AF8	**AF9**	**AF10**	**AF11**	**AF12**	**AF13**	**AF14**	**AF15**
	-	-	SPI1_SCK	-	I^2C_SDA	TIM3_CH1	-	-
PA3	**AF0**	**AF1**	**AF2**	**AF3**	**AF4**	**AF5**	**AF6**	**AF7**
	-	USART1_RX	-	-	USART2_RX	-	-	EVENTOUT
	AF8	**AF9**	**AF10**	**AF11**	**AF12**	**AF13**	**AF14**	**AF15**
	-	-	SPI1_MOSI	-	I^2C_SCL	TIM1_CH1	-	-
PA4	**AF0**	**AF1**	**AF2**	**AF3**	**AF4**	**AF5**	**AF6**	**AF7**
	SPI1_NSS	USART1_CK	-	-	TIM14_CH1	USART2_CK	-	EVENTOUT
	AF8	**AF9**	**AF10**	**AF11**	**AF12**	**AF13**	**AF14**	**AF15**
	-	USART2_TX	-	-	-	TIM3_CH3	-	RTC_OUT
PA5	**AF0**	**AF1**	**AF2**	**AF3**	**AF4**	**AF5**	**AF6**	**AF7**
	SPI1_SCK	-	-	-	-	LPTIM1_ETR	-	EVENTOUT
	AF8	**AF9**	**AF10**	**AF11**	**AF12**	**AF13**	**AF14**	**AF15**
	-	USART2_RX	-	-	-	TIM3_CH2	-	MCO
PA6	**AF0**	**AF1**	**AF2**	**AF3**	**AF4**	**AF5**	**AF6**	**AF7**
	SPI1_MISO	TIM3_CH1	TIM1_BKIN	-	-	TIM16_CH1	-	COMP1_OUT
	AF8	**AF9**	**AF10**	**AF11**	**AF12**	**AF13**	**AF14**	**AF15**
	USART1_CK	-	-	-	-	-	-	RTC_OUT
PA7	**AF0**	**AF1**	**AF2**	**AF3**	**AF4**	**AF5**	**AF6**	**AF7**
	SPI1_MOSI	TIM3_CH2	TIM1_CH1N	-	TIM14_CH1	TIM17_CH1	EVENTOUT	COMP2_OUT
	AF8	**AF9**	**AF10**	**AF11**	**AF12**	**AF13**	**AF14**	**AF15**
	USART1_TX	USART2_TX	SPI1_MISO	-	I^2C_SDA	-	-	-
PA8	**AF0**	**AF1**	**AF2**	**AF3**	**AF4**	**AF5**	**AF6**	**AF7**
	-	USART1_CK	TIM1_CH1	-	USART2_CK	MCO	-	EVENTOUT
	AF8	**AF9**	**AF10**	**AF11**	**AF12**	**AF13**	**AF14**	**AF15**
	USART1_RX	USART2_RX	SPI1_MOSI	-	I^2C_SCL	-	-	-
PA9	**AF0**	**AF1**	**AF2**	**AF3**	**AF4**	**AF5**	**AF6**	**AF7**
	-	USART1_TX	TIM1_CH2	-	USART2_TX	MCO	I^2C_SCL	EVENTOUT
	AF8	**AF9**	**AF10**	**AF11**	**AF12**	**AF13**	**AF14**	**AF15**
	USART1_RX	-	SPI1_SCK	-	I^2C_SDA	TIM1_BKIN	-	-
PA10	**AF0**	**AF1**	**AF2**	**AF3**	**AF4**	**AF5**	**AF6**	**AF7**
	-	USART1_RX	TIM1_CH3	-	USART2_RX	TIM17_BKIN	I^2C_SDA	EVENTOUT
	AF8	**AF9**	**AF10**	**AF11**	**AF12**	**AF13**	**AF14**	**AF15**
	USART1_TX	-	SPI1_NSS	-	I^2C_SCL	-	-	-
PA11	**AF0**	**AF1**	**AF2**	**AF3**	**AF4**	**AF5**	**AF6**	**AF7**
	SPI1_MISO	USART1_CTS	TIM1_CH4	-	USART2_CTS	EVENTOUT	I^2C_SCL	COMP1_OUT
PA12	**AF0**	**AF1**	**AF2**	**AF3**	**AF4**	**AF5**	**AF6**	**AF7**
	SPI1_MOSI	USART1_RTS	TIM1_ETR	-	USART2_RTS	EVENTOUT	I^2C_SDA	COMP2_OUT
PA13	**AF0**	**AF1**	**AF2**	**AF3**	**AF4**	**AF5**	**AF6**	**AF7**
	SWDIO	IR_OUT	-	-	-	-	-	EVENTOUT
	AF8	**AF9**	**AF10**	**AF11**	**AF12**	**AF13**	**AF14**	**AF15**
	USART1_RX	-	SPI1_MISO	-	-	TIM1_CH2	-	MCO
PA14	**AF0**	**AF1**	**AF2**	**AF3**	**AF4**	**AF5**	**AF6**	**AF7**
	SWCLK	USART1_TX	-	-	USART2_TX	-	-	EVENTOUT
	AF8	**AF9**	**AF10**	**AF11**	**AF12**	**AF13**	**AF14**	**AF15**
	-	-	-	-	-	-	-	MCO
PA15	**AF0**	**AF1**	**AF2**	**AF3**	**AF4**	**AF5**	**AF6**	**AF7**

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
	SPI1_NSS	USART1_RX	-	-	USART2_RX	-	-	EVENTOUT

3.2. Port B multiplexing function mapping

Table 3-7 Port B multiplexing function mapping

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PB0	SPI1_NSS	TIM3_CH3	TIM1_CH2N	-	-	EVENTOUT	-	COMP1_OUT
PB1	**AF0**	**AF1**	**AF2**	**AF3**	**AF4**	**AF5**	**AF6**	**AF7**
	TIM14_CH1	TIM3_CH4	TIM1_CH3N	-	-	-	-	EVENTOUT
PB2	**AF0**	**AF1**	**AF2**	**AF3**	**AF4**	**AF5**	**AF6**	**AF7**
	USART1_RX	-	-	USART2_RX	-	-	-	-
PB3	**AF0**	**AF1**	**AF2**	**AF3**	**AF4**	**AF5**	**AF6**	**AF7**
	SPI1_SCK	TIM1_CH2	-	USART1_RTS	USART2_RTS	-	-	EVENTOUT
PB4	**AF0**	**AF1**	**AF2**	**AF3**	**AF4**	**AF5**	**AF6**	**AF7**
	SPI1_MISO	TIM3_CH1	-	USART1_CTS	USART2_CTS	TIM17_BKIN	-	EVENTOUT
PB5	**AF0**	**AF1**	**AF2**	**AF3**	**AF4**	**AF5**	**AF6**	**AF7**
	SPI1_MOSI	TIM3_CH2	TIM16_BKIN	USART1_CK	USART2_CK	LPTIM_IN1	-	COMP1_OUT
PB6	**AF0**	**AF1**	**AF2**	**AF3**	**AF4**	**AF5**	**AF6**	**AF7**
	USART1_TX	TIM1_CH3	TIM16_CH1N	-	USART2_TX	LPTIM_ETR	I^2C_SCL	EVENTOUT
PB7	**AF0**	**AF1**	**AF2**	**AF3**	**AF4**	**AF5**	**AF6**	**AF7**
	USART1_RX	-	TIM17_CH1N	-	USART2_RX	-	I^2C_SDA	EVENTOUT
PB8	**AF0**	**AF1**	**AF2**	**AF3**	**AF4**	**AF5**	**AF6**	**AF7**
	-	-	TIM16_CH1	-	USART2_TX	-	I^2C_SCL	EVENTOUT
	AF8	**AF9**	**AF10**	**AF11**	**AF12**	**AF13**	**AF14**	**AF15**
	USART1_TX	-	-	-	I^2C_SDA	TIM17_CH1	-	IR_OUT

3.3. Port F multiplexing function mapping

Table 3-8 Port F multiplexing function mapping

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PF0-OSC_IN	-	-	TIM14_CH1	-	USART2_RX	-	-	-
	AF8	**AF9**	**AF10**	**AF11**	**AF12**	**AF13**	**AF14**	**AF15**
	USART1_RX	USART2_TX	-	-	I^2C_SDA	-	-	-
PF1_OSC_OUT	**AF0**	**AF1**	**AF2**	**AF3**	**AF4**	**AF5**	**AF6**	**AF7**
	-	-	-	-	USART2_TX	-	-	-
	AF8	**AF9**	**AF10**	**AF11**	**AF12**	**AF13**	**AF14**	**AF15**
	USART1_TX	USART2_RX	SPI1_NSS	-	I^2C_SCL	TIM14_CH1	-	-
PF2-NRST	**AF0**	**AF1**	**AF2**	**AF3**	**AF4**	**AF5**	**AF6**	**AF7**
	-	-	-	-	USART2_RX	-	MCO	-
PF3	**AF0**	**AF1**	**AF2**	**AF3**	**AF4**	**AF5**	**AF6**	**AF7**
	USART1_TX	-	-	-	USART2_TX	-	-	-
	AF8	**AF9**	**AF10**	**AF11**	**AF12**	**AF13**	**AF14**	**AF15**
	-	-	SPI1_NSS	-	-	TIM3_CH3	-	RTC_OUT
PF4-BOOT0	**AF0**	**AF1**	**AF2**	**AF3**	**AF4**	**AF5**	**AF6**	**AF7**
	-	-	-	-	-	-	-	-

4. Memory Map

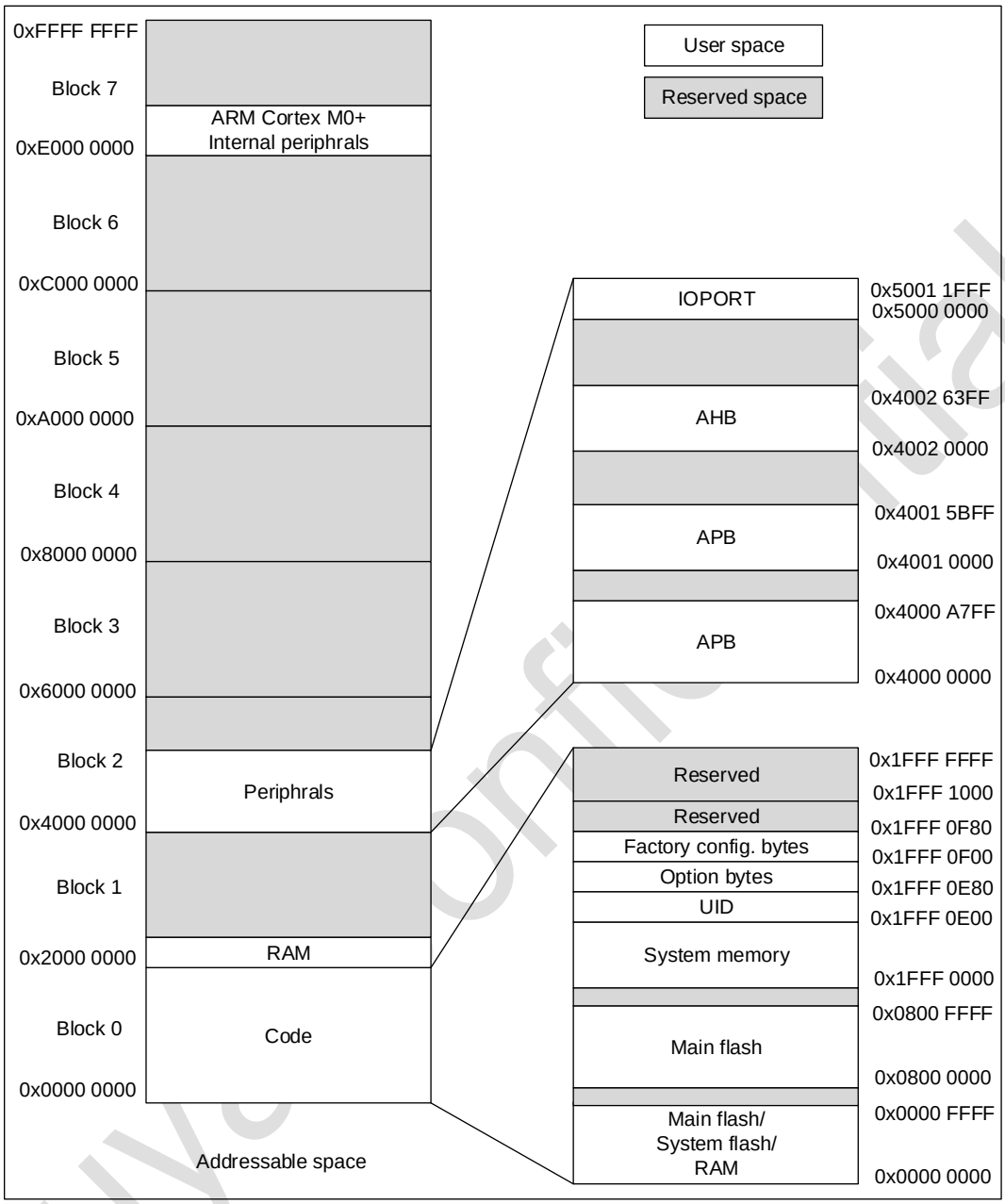


Figure 4-1 Memory map

Table 4-1 Memory address

Type	Boundary Address	Size	Memory Area	Description
SRAM	0x2000 1 000-0x3FFF FFFF	512 Mbytes	Reserved	
	0x2000 0000-0x2000 1FFF	8 Kbytes	SRAM	Depending on the hardware, the SRAM is up to 8 kBytes
Code	0x1FFF 1000-0x1FFF FFFF	4 Kbytes	Reserved	
	0x1FFF 0F80-0x1FFF 0FFF	128 Bytes	Reserved	

Type	Boundary Address	Size	Memory Area	Description
	0x1FFF 0F00-0x1FFF 0F7F	128 Bytes	Factory config	Store HSI triming data, flash erasing time configuration parameters
	0x1FFF 0E80-0x1FFF 0EFF	128 Bytes	Option bytes	Option bytes
	0x1FFF 0E00-0x1FFF 0E7F	128 Bytes	UID	Unique ID
	0x1FFF 0000-0x1FFF 0DFF	3.5 Kbytes	System memory	Store the boot loader
	0x0800 8000-0x1FFE FFFF	384 Mbytes	Reserved	
	0x0800 0000-0x0800 FFFF	64 Kbytes	Main flash memory	
	0x0001 0000-0x07FF FFFF	8 Mbytes	Reserved	
	0x0000 0000-0x0000 FFFF	64 Kbytes	According to the Boot configuration: 1) Main flash memory 2) System memory 3) SRAM	

1. Except for 0x1FFF 0E00-0x1FFF 0E7F, the above spaces are marked as reserved spaces, which cannot be written and read as 0 with response error.

Table 4-2 Peripheral register address

Bus	Boundary Address	Size	Peripheral
	0xE000 0000-0xE00F FFFF	1 Mbytes	M0+
IOPORT	0x5000 1800-0x5FFF FFFF	-	Reserved (1)
	0x5000 1400-0x5000 17FF	1 Kbytes	GPIOF
	0x5000 1000-0x5000 13FF	-	Reserved
	0x5000 0C00-0x5000 0FFF	-	Reserved
	0x5000 0C00-0x5000 0FFF	-	Reserved
	0x5000 0400-0x5000 07FF	1 Kbytes	GPIOB
	0x5000 0000-0x5000 03FF	1 Kbytes	GPIOA
AHB	0x4002 3400-0x4FFF FFFF	-	Reserved
	0x4002 300C-0x4002 33FF	1 Kbytes	Reserved
	0x4002 3000-0x4002 3008		CRC
	0x4002 2400-0x4002 2FFF	-	Reserved
	0x4002 2124-0x4002 23FF	1 Kbytes	Reserved
	0x4002 2000-0x4002 2120		Flash
	0x4002 1C00-0x4002 1FFF	-	Reserved
	0x4002 1888-0x4002 1BFF	1 Kbytes	Reserved
	0x4002 1800-0x4002 1884		EXTI(2)
	0x4002 1400-0x4002 17FF	-	Reserved
	0x4002 1064-0x4002 13FF	1 Kbytes	Reserved
	0x4002 1000-0x4002 1060		RCC(2)
	0x4002 0C00-0x4002 0FFF	-	Reserved
	0x4002 0040-0x4002 03FF	1 Kbytes	Reserved
	0x4002 0000-0x4002 003C		DMA

Bus	Boundary Address	Size	Peripheral
APB	0x4001 5C00-0x4001 FFFF	-	Reserved
	0x4001 5880-0x4001 5BFF	1 Kbytes	Reserved
	0x4001 5800-0x4001 587F		DBG
	0x4001 4C00-0x4001 57FF	-	Reserved
	0x4001 4850-0x4001 4BFF	1 Kbytes	Reserved
	0x4001 4800-0x4001 484C		TIM17
	0x4001 4450-0x4001 47FF	1 Kbytes	Reserved
	0x4001 4400-0x4001 404C		TIM16
	0x4001 3C00-0x4001 43FF	-	Reserved
	0x4001 381C-0x4001 3BFF	1 Kbytes	Reserved
	0x4001 3800-0x4001 3018		USART1
	0x4001 3400-0x4001 37FF	-	Reserved
	0x4001 3010-0x4001 33FF	1 Kbytes	Reserved
	0x4001 3000-0x4001 300C		SPI1
	0x4001 2C50-0x4001 2FFF	1 Kbytes	Reserved
	0x4001 2C00-0x4001 2C4C		TIM1
	0x4001 2800-0x4001 2BFF	-	Reserved
	0x4001 270C-0x4001 27FF	1 Kbytes	Reserved
	0x4001 2400-0x4001 2708		ADC
	0x4001 0400-0x4001 23FF	-	Reserved
	0x4001 0220-0x4001 03FF	1 Kbytes	Reserved
	0x4001 0200-0x4001 021F		COMP1 and COMP2
	0x4001 0000-0x4001 01FF		SYSCFG
	0x4000 B400-0x4000 FFFF	-	Reserved
	0x4000 B000-0x4000 B3FF	-	Reserved
	0x4000 8400-0x4000 AFFF	-	Reserved
	0x4000 8000-0x4000 83FF	-	Reserved
	0x4000 7C28-0x4000 7FFF	1 Kbytes	Reserved
	0x4000 7C00-0x4000 7C24		LPTIM
	0x4000 7400-0x4000 7BFF	-	Reserved
	0x4000 7018-0x4000 73FF	1 Kbytes	Reserved
	0x4000 7000-0x4000 7014		PWR(3)
	0x4000 5800-0x4000 6FFF	-	Reserved
	0x4000 5434-0x4000 57FF	1 Kbytes	Reserved
	0x4000 5400-0x4000 5430		I^2C
	0x4000 4800-0x4000 53FF	-	Reserved
	0x4000 441C-0x4000 47FF	1 Kbytes	Reserved
	0x4000 4400-0x4000 4418		USART2
	0x4000 3C00-0x4000 43FF	-	Reserved
	0x4000 3800-0x4000 3BFF	1 Kbytes	Reserved

Bus	Boundary Address	Size	Peripheral
	0x4000 3400-0x4000 37FF	-	Reserved
	0x4000 3014-0x4000 33FF	1 Kbytes	Reserved
	0x4000 3000-0x4000 0010		IWDG
	0x4000 2C0C-0x4000 2FFF	1 Kbytes	Reserved
	0x4000 2C00-0x4000 2C08		WWDG
	0x4000 2830-0x4000 2BFF	1 Kbytes	Reserved
	0x4000 2800-0x4000 282C		RTC(3)
	0x4000 2400-0x4000 27FF	-	Reserved
	0x4000 2054-0x4000 23FF	1 Kbytes	Reserved
	0x4000 2000-0x4000 0050		TIM14
	0x4000 1800-0x4000 1FFF	-	Reserved
	0x4000 1400-0x4000 17FF	-	Reserved
	0x4000 1000-0x4000 13FF	-	Reserved
	0x4000 0800-0x4000 0FFF	-	Reserved
	0x4000 0450-0x4000 07FF	1 Kbytes	Reserved
	0x4000 0400-0x4000 044C		TIM3
	0x4000 0000-0x4000 03FF	-	Reserved

1. The address space marked as Reserved by AHB in the above table cannot be written, read is 0, and a hardfault is generated. The address space marked as Reserved by APB cannot be written, read back as 0, but no hardfault will be generated.
2. Not only supports 32 bits word access, but also supports halfword and byte access.
3. Not only supports 32 bits word access, but also supports halfword access.

5. Electrical characteristics

5.1. Test conditions

All voltages are referenced to V_{SS} unless otherwise specified.

5.1.1. Min and Max

Unless otherwise specified, the chip is screened by mass production testing at ambient temperature T_A =25°C and T_A =$T_{A(max)}$, guaranteed to reach the minimum value and maximum value under the worst ambient temperature, supply voltage and clock frequency conditions.

Based on electrical characterization results, design simulations, and/or process parameters noted below the table, not tested in production. Minimum and maximum values are referenced to sample testing and averaged plus or minus three times the standard deviation.

5.1.2. Typical value

Unless otherwise specified, typical data is based on T_A =25°C and V_{CC} = 3.3 V. These data are for design guidance only and have not been tested.

Typical ADC accuracy values are obtained by sampling a standard batch, tested under all temperature ranges, and 95% of the chip error is less than or equal to the given value.

5.2. Absolute maximum ratings

If the applied voltage exceeds the absolute maximum value given in the table below, it may cause permanent damage to the chip. Only the strength ratings that can be tolerated are listed here, and it does not imply that the functional operation of the device is correct under these conditions. Operating under maximum conditions for a long time may affect the reliability of the chip.

Table 5-1 Voltage characteristics (1)

Symbol	Describe	Minimum	Maximum	Unit
V_{CC}	External mains power supply	-0.3	6.25	V
V_{IN}	Input voltage of other pins	-0.3	V_{CC} + 0.3	V

1. Power supply V_{CC} and ground V_{SS} pins must always be connected to the external power supply within the allowable range.

Table 5-2 Current characteristics

Symbol	Describe	Maximum	Unit
I_{VCC}	Flowing into V_{CC} pin (supply current) (1)	100	mA
I_{VSS}	Total current flowing out of V_{SS} pin (outflow current) (1)	100	

$I_{IO(PIN)}$	Output sink current of COM IO	20	
	Source current for all IOs	- 20	

1. Power supply V_{CC} and ground V_{SS} pins must always be connected to the external power supply within the allowable range.

Table 5-3 Temperature characteristics

Symbol	Describe	Condition	Value	Unit
T_{STG}	Storage temperature range		- 65 ~ + 150	℃
T_O	Range of operating temperature	x6 version	- 40 ~ + 85	℃
		x7 version	- 40 ~ + 105	

5.3. Operating conditions

5.3.1. General operating conditions

Table 5-4 General operating conditions

Symbol	Parameter	Condition	Minimum	Maximum	Unit
f_{HCLK}	Internal AHB clock frequency	-	0	32	MHz
f_{PCLK}	Internal APB Clock Frequency	-	0	32	MHz
V_{CC}	Standard operating voltage	x6 version	1.7	5.5	V
		x7 version	2.0	5.5	
V_{IN}	IO input voltage	-	-0.3	V_{CC}+0.3	V
T_A	Ambient temperature	x6 version	-40	85	℃
		x7 version	-40	105	
T_J	Junction temperature	x6 version	-40	90	℃
		x7 version	-40	110	

5.3.2. Power on and down operating conditions

Table 5-5 Power on and Power down Operating Conditions

Symbol	Parameter	Condition	Minimum	Maximum	Unit
t_{VCC}	V_{CC} rise rate	-	0	∞	us/V
	V_{CC} fall rate	-	20	∞	

5.3.3. Embedded reset and LVD module features

Table 5-6 Embedded Reset Module Features

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
$t_{RSTTEMPO}$(1)	Reset time	-	-	4.0	7.5	ms
$V_{POR/PDR}$	POR/PDR reset threshold	rising edge	1.5 0 (2)	1.60	1.70	V
		falling edge	1.45 (1)	1.55	1.65 (2)	V
V_{BOR1}	BOR threshold 1	rising edge	1.70 (2)	1.80	1.90	V
		falling edge	1.60	1.70	1.80 (2)	V

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
V_{BOR2}	BOR threshold 2	rising edge	1.90 (2)	2.00	2.10	V
		falling edge	1.80	1.90	2.00 (2)	V
V_{BOR3}	BOR threshold 3	rising edge	2.10 (2)	2.20	2.30	V
		falling edge	2.00	2.10	2.20 (2)	V
V_{BOR4}	BOR threshold 4	rising edge	2.30 (2)	2.40	2.50	V
		falling edge	2.20	2.30	2.40 (2)	V
V_{BOR5}	BOR threshold 5	rising edge	2.50 (2)	2.60	2.70	V
		falling edge	2.40	2.50	2.60 (2)	V
V_{BOR6}	BOR threshold 6	rising edge	2.70 (2)	2.80	2.90	V
		falling edge	2.60	2.70	2.80 (2)	V
V_{BOR7}	BOR threshold 7	rising edge	2.90 (2)	3.00	3.10	V
		falling edge	2.80	2.90	3.00 (2)	V
V_{BOR8}	BOR threshold 8	rising edge	3.10 (2)	3.20	3.30	V
		falling edge	3.00	3.10	3.20 (2)	V
V_{PVD0}	PVD threshold 0	rising edge	1.70 (2)	1.80	1.90	V
		falling edge	1.60	1.70	1.80 (2)	V
V_{PVD1}	PVD Threshold 1	rising edge	1.90 (2)	2.00	2.10	V
		falling edge	1.80	1.90	2.00 (2)	V
V_{PVD2}	PVD Threshold 2	rising edge	2.10 (2)	2.20	2.30	V
		falling edge	2.00	2.10	2.20 (2)	V
V_{PVD3}	PVD Threshold 3	rising edge	2.30 (2)	2.40	2.50	V
		falling edge	2.20	2.30	2.40 (2)	V
V_{PVD4}	PVD Threshold 4	rising edge	2.50 (2)	2.60	2.70	V
		falling edge	2.40	2.50	2.60 (2)	V
V_{PVD5}	PVD threshold 5	rising edge	2.70 (2)	2.80	2.90	V
		falling edge	2.60	2.70	2.80 (2)	V
V_{PVD6}	PVD threshold 6	rising edge	2.90 (2)	3.00	3.10	V
		falling edge	2.80	2.90	3.00 (2)	V
V_{PVD7}	PVD threshold 7	rising edge	3.10 (2)	3.20	3.30	V
		falling edge	3.00	3.10	3.20 (2)	V
$V_{POR\_PDR\_hyst}$(1)	POR / PDR hysteresis voltage	-	-	50	-	mV
$V_{PVD\_BOR\_hyst}$(1)	PVD hysteresis voltage	-	-	100	-	mV
$I_{DD(PVD)}$	PVD power consumption	-	-	0.6	-	uA
$I_{DD(BOR)}$	BOR power consumption	-	-	0.6	-	uA

1. Guaranteed by design, not tested in production.
2. Data is based on assessment results and is not tested in production.

5.3.4. Operating current characteristics

Table 5-7 Run mode current

Symbol	Condition						Typical (1)	Maxi-mum	Unit
	System clock	Frequency	Code	Run	Peripheral clock	FLASH sleep			
I_{DD}(run)	HSI	24 MHz	While	Flash	ON	DISABLE	1.5	-	mA

Symbol	Condition						Typical (1)	Maxi-mum	Unit
	System clock	Frequency	Code	Run	Peripheral clock	FLASH sleep			
			(1)		OFF	DISABLE	0.9	-	
		16 MHz			ON	DISABLE	1.1	-	
					OFF	DISABLE	0.7	-	
		8 MHz			ON	DISABLE	0.7	-	
					OFF	DISABLE	0.5	-	
		4 MHz			ON	DISABLE	0.5	-	
					OFF	DISABLE	0.35	-	
	LSI	32.768 kHz			ON	DISABLE	170	-	
					OFF	DISABLE	170	-	uA
		32.768 kHz			ON	ENABLE	95	-	
					OFF	ENABLE	95	-	

1. Data is based on assessment results and is not tested in production.

Table 5-8 Sleep mode current

Symbol	Condition				Typical (1)	Maximum	Unit
	System clock	Frequency	Peripheral clock	FLASH sleep			
I_{DD}(sleep)	HSI	24 MHz	ON	DISABLE	1	-	mA
			OFF	DISABLE	0.6	-	
		16 MHz	ON	DISABLE	0.75	-	
			OFF	DISABLE	0.5	-	
		8 MHz	ON	DISABLE	0.5	-	
			OFF	DISABLE	0.35	-	
		4 MHz	ON	DISABLE	0.4	-	
			OFF	DISABLE	0.35	-	
	LSI	32.768 kHz	ON	DISABLE	170	-	
			OFF	DISABLE	170	-	uA
		32.768 kHz	ON	ENABLE	95	-	
			OFF	ENABLE	96	-	

1. Data is based on assessment results and is not tested in production.

Table 5-9 Stop mode current

Symbol	Condition					Typical (1)	Maximum	Unit
	V_{CC}	V_{DD}	MR/ LPR	LSI	Peripheral clock			
I_{DD}(stop)	V_{CC}=1.7 ~ 5.5 V	1.2 V	MR	-	-	70	-	uA
		1.2 V	LPR	ON	RTC+IWDG+LPTIM	6	-	
					IWDG	6	-	
					LPTIM	6	-	
					RTC	6	-	

Symbol	Condition					Typical (1)	Maximum	Unit
	V_{CC}	V_{DD}	MR/ LPR	LSI	Peripheral clock			
				OFF	No	6	-	
		1.0 V		ON	RTC+IWDG+LPTIM	4.5	-	
					IWDG	4.5	-	
					LPTIM	4.5	-	
					RTC	4.5	-	
				OFF	No	4.5	-	

1. Data is based on assessment results and is not tested in production.

5.3.5. Low power mode wake-up time

Table 5-10 Low power mode wake-up time

Symbol	Parameters(1)		Condition		Typical(2)	maximum	Unit
$t_{WUSLEEP}$	Wake-up time from sleep		-		1.65	-	us
t_{WUSTOP}	Wake-up time from stop	Powered by MR	Execute program in Flash, HSI (24 Mhz) as system clock		3.5	-	us
		Powered by LPR	Execute program in Flash, HSI as system clock	V_{DD}=1.2 V	6	-	
				V_{DD}=1.0 V	6	-	

1. The wake-up time is measured from the wake-up time until the first instruction is read by the user program.
2. Data is based on assessment results and is not tested in production.

5.3.6. External clock source characteristics

5.3.6.1. External high-speed clock

In the bypass mode of HSE (the HSEBYP of RCC_CR is set), when the high-speed start-up circuit in the chip stops working, the corresponding IO is used as a standard GPIO.

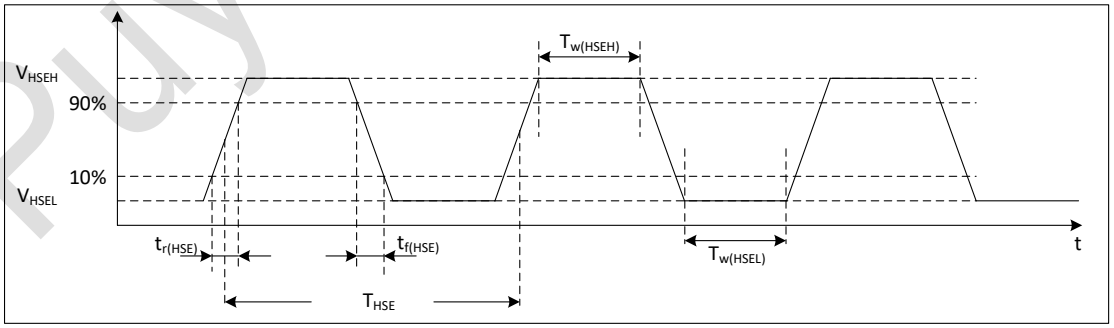


Figure 5-1 External high-speed clock timing diagram

Table 5-11 External high-speed clock features

Symbol	Parameters(1)	Minimum	Typical	Maximum	Unit
f_{HSE_ext}	User external clock frequency	0	8	32	MHz

Symbol	Parameters(1)	Minimum	Typical	Maximum	Unit
V_{HSEH}	Input pin high level voltage	$0.7V_{CC}$	-	V_{CC}	V
V_{HSEL}	Input pin low level voltage	Vss	-	$0.3V_{CC}$	
$t_{W(HSEH)}$ $t_{W(HSEL)}$	Enter high or low time	1 5	-	-	ns
$t_{r(HSE)}$ $t_{f(HSE)}$	Enter the rise/fall time	-	-	20	ns

1. Guaranteed by design, not tested in production.

5.3.6.2. External high-speed crystal

An external 4~32 MHz crystal/ceramic resonator. In the application, the crystal and load capacitors should be as close as possible to the pins to minimize output distortion and start-up settling time.

Table 5-12 External high-speed crystal characteristics

Symbol	Parameter	Condition(1)	Minimum(2)	Typical	Maximum(2)	Unit
f_{OSC_IN}	Oscillation frequency	-	4	-	32	MHz
I_{DD}(4)	HSE power consumption	During startup	-	-	5.5	mA
		V_{CC}=3 V, Rm=30 Ω, C_L=10 pF@8 MHz	-	0.58	-	
		V_{CC}=3 V,Rm=45Ω, C_L=10 pF@8 MHz	-	0.59	-	
		V_{CC}=3 V,Rm=30Ω, C_L=5 pF@32MHz	-	0.89	-	
		V_{CC}=3 V,Rm=30Ω, C_L=10 pF@32 MHz	-	1.10	-	
		V_{CC}=3 V,Rm=30Ω, C_L=20 pF@32 MHz	-	1.90	-	
$t_{SU\ (HSE)}$ (3) (4)	Start Time	f_{OSC_IN}=32 MHz	-	3	-	ms
		f_{OSC_IN}=4 MHz	-	15	-	

1. Crystal/ceramic resonator characteristics are based on the manufacturer datasheet.
2. Guaranteed by design, not tested in production.
3. $t_{SU(HSE)}$ is the start-up time from enable (by software) to the clock oscillation reaches stability, measured for a standard crystal/resonator, which can vary greatly from one crystal/resonator to another .
4. Data is based on assessment results and is not tested in production.

5.3.7. Internal high frequency clock source HSI characteristics

Table 5-13 Internal high frequency clock source characteristics

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
f_{HSI}	HSI frequency	T_A=25°C,V_{CC}=3.3 V	23.83(2)	24	24.17(2)	MHz
			21.97(2)	22.12	22.27(2)	
			15.89(2)	16	16.11(2)	
			7.94(2)	8	8.06(2)	

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
			3.97(2)	4	4.03(2)	
$\Delta_{Temp(HSI)}$	HSI frequency temperature drift	T_A=0 ~ 85°C	-2(2)	-	2(2)	%
		T_A=-40 ~ 85°C	-4(2)	-	2(2)	
		T_A=-40 ~ 105°C	-4(2)	-	2.5(2)	
f_{TRIM}(1)	HSI fine-tuning accuracy	-	-	0.1	-	%
D_{HSI}(1)	Duty cycle	-	45(1)		55(1)	%
$t_{Stab(HSI)}$	HSI stabilization time	-	-	2	4(1)	us
$I_{DD(HSI)}$ (2)	HSI power consumption	4 MHz	-	100	-	uA
		8 MHz	-	105	-	
		16 MHz	-	150	-	
		22.12 MHz, 24 MHz	-	180	-	

1. Guaranteed by design, not tested in production.
2. Data is based on assessment results and is not tested in production.

5.3.8. Internal low frequency clock source LSI characteristics

Table 5-14 Internal low frequency clock characteristics

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
f_{LSI}	LSI frequency	T_A=25°C,V_{CC}=3.3V	-1	-	+1	%
$\Delta_{Temp(LSI)}$	LSI frequency tempera-ture drift	T_A=0 ~ 70°C	-10(2)	-	10(2)	%
		T_A=-40 ~ 105°C	-20(2)	-	20(2)	
f_{TRIM}(1)	LSI fine-tuning accuracy	-	-	0.2	-	%
$t_{Stab(LSI)}$ (1)	LSI stabilization time	-	-	150	-	us
$I_{DD(LSI)}$ (1)	LSI power consumption	-	-	210	-	nA

1. Guaranteed by design, not tested in production.
2. Data is based on assessment results and is not tested in production.

5.3.9. Memory characteristics

Table 5-15 Memory characteristics

Symbol	Parameter	Condition	Typical	Maximum(1)	Unit
t_{prog}	Page program	-	1.0	1.5	ms
t_{ERASE}	Page/sector/mass erase	-	3.0	4.5	ms
I_{DD}	Page programe	-	2.1	2.9	mA
	Page/sector/mass erase	-	2.1	2.9	

1. Guaranteed by design, not tested in production.

Table 5-16 Memory erase times and data retention

Symbol	Parameter	Condition	Minimum(1)	Unit
N_{END}	Erase and write times	T_A = -40 ~ 105℃	100	kcycle
		T_A = 85 ~ 105℃	10	
t_{RET}	Data retention period	10 kcycle T_A = 55℃	20	Year

1. Data is based on assessment results and is not tested in production.

5.3.10. EFT characteristics

Table 5-17 EFT characteristics

Symbol	Parameter	Condition	Grade	Typical	Unit
EFT to Power	-	IEC61000-4-4	A	4	KV

5.3.11. ESD & LU Characteristics

Table 5-18 ESD & LU characteristics

Symbol	Parameter	Condition	Typical	Unit
$V_{ESD(HBM)}$	Static Discharge Voltage (human body model)	ESDA/JEDEC JS-001-2017	6	KV
$V_{ESD(CDM)}$	Static Discharge Voltage (charging equipment model)	ESDA/JEDEC JS-002-2018	1	KV
$V_{ESD(MM)}$	Static discharge voltage (machine model)	JESD22-A115C	200	V
LU	Static Latch-Up	JESD78E	200	mA

5.3.12. Port characteristics

Table 5-19 IO static characteristics

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
V_{IH}	Input high level voltage	T_A = -40 ~105℃	0.7V_{CC}	-	-	V
V_{IL}	Input low level voltage	T_A = -40 ~105℃	-	-	0.3V_{CC}	V
V_{hys}(1)	Schmitt hysteresis voltage	-	-	200	-	mV
I_{lkg}	Input leakage current	-	-		1	uA
R_{PU}	Pull-up resistor	-	30	50	70	kΩ
R_{PD}	Pull-down resistor	-	30	50	70	kΩ
C_{IO}(1)	Pin capacitance	-	-	5	-	pF

1. Guaranteed by design, not tested in production.

Table 5-20 Output Voltage Characteristics

symbol	Parameters (1)	condition	Minimum	Maximum	unit
V_{OL}	COM IO output low level	IOL = 8 mA, V_{CC} ≥ 2.7 V	-	0.4	V
		IOL = 4 mA, V_{CC} = 1.8 V	-	0.5	
V_{OH}	COM IO output high level	IOH = 8 mA, V_{CC} ≥ 2.7 V	V_{CC}–0.4	-	V
		IOH = 4 mA, V_{CC} = 1.8 V	V_{CC}–0.5	-	

1. IO types can refer to the terms and symbols defined by the pins.

5.3.13. NRST pin characteristics

Table 5-21 NRST pin characteristics

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
V_{IH}	Input high level voltage	T_A = -40 ~105℃	0.7V_{CC}	-	-	V
V_{IL}	Input low level voltage	T_A = -40 ~105℃	-	-	0.2V_{CC}	V
V_{hys}(1)	Schmitt hysteresis voltage	-	-	300	-	mV
I_{lkg}	Input leakage current	-	-	-	1	uA
R_{PU}(1)	Pull-up resistor	-	30	50	70	kΩ
R_{PD}(1)	Pull-down resistor	-	30	50	70	kΩ
C_{IO}	Pin capacitance	-	-	5	-	pF

1. Guaranteed by design, not tested in production.

5.3.14. ADC characteristics

Table 5-22 ADC characteristics

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
I_{DD}	Power consumption	@0.75 MSPS	-	1.0	-	mA
C_{IN}(1)	Internal sample and hold capacitors	-	-	5	-	pF
F_{ADC}	Convert clock frequency	V_{CC}=1.7~2.3 V	1	4	6(2)	MHz
		V_{CC}=2.3~5.5 V	1	8	12(2)	
t_{samp}(1)	-	V_{CC}=1.7~2.3 V	0.2	-	-	us
	-	V_{CC}=2.3~5.5 V	0.1	-	-	
t_{conv}(1)	-	-	-	12*Tclk	-	
t_{eoc}(1)	-	-	-	0.5*Tclk	-	
DNL(2)	-	-	-	±2	-	LSB
INL(2)	-	-	-	±3	-	LSB
Offset(2)	-	-	-	±2	-	LSB

1. Guaranteed by design, not tested in production.
2. Data is based on assessment results and is not tested in production.

5.3.15. Comparator characteristics

Table 5-23 Comparator characteristics (1)

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
V_{IN}	Input voltage range	-	0	-	V_{CC}	V
V_{BG}	Scale input voltage	-	V_{REFINT}			V

Symbol	Parameter	Condition		Minimum	Typical	Maximum	Unit
V_{SC}	Scaler offset voltage	-		-	±5	±10	mV
$I_{DD(SCALER)}$	Scaler static consumption	BRG_EN=0(bridge disable)		-	200	300	nA
		BRG_EN=1(bridge enable)		-	0.8	1	uA
t_{START_SCALER}	Scaler startup time	-		-	100	200	us
t_{START}	Startup time to reach propagation delay specification	High-speed mode		-	-	5	us
		Medium-speed mode		-	-	15	
t_D	Propagation delay	200 mV step; 100 mV overdrive	High-speed mode	-	30	50	ns
			Medium-speed mode	-	0.3	0.6	us
		>200 mV step;100 mV overdrive	High-speed mode	-	-	10	us
			Medium-speed mode	-	-	1.2	ns
Voffset	Offset error	-		-	±5	-	mV
Vhys	Hysteresis	No hysteresis		-	0	-	mV
		Low hysteresis		-	10	-	
		Medium hysteresis		-	20	-	
		High hysteresis		-	30	-	
I_{DD}	Consumption	Medium-speed mode; No deglitcher	Static	-	5	-	uA
			With 50 kHz and ±100 mv overdrive square signal	-	6	-	uA
		Medium-speed mode With deglitcher	Static	-	7	-	uA
			With 50 kHz and ±100 mv overdrive square signal	-	8	-	uA
		High-speed mode; No deglitcher	Static	-	250	-	uA
			With 50 kHz and ±100 mv overdrive square signal	-	250	-	uA

1. Guaranteed by design, not tested in production.

5.3.16. Temperature sensor characteristics

Table 5-24 Temperature sensor characteristics

Symbol	Parameter	Minimum	Typical	Maximum	Unit
T_L(1)	V_{TS} linearity with temperature	-	±1	±2	℃
Avg_Slope(1)	Average slope	2.3	2.5	2.7	mV/℃
V_{30}	Voltage at 30℃(±5℃)	0.742	0.76	0.785	V

Symbol	Parameter	Minimum	Typical	Maximum	Unit
t_{START}(1)	Start-up time entering in continuous mode	-	70	120	us
t_{S_temp}(1)	ADC sampling time when reading the temperature	9	-	-	us

1. Guaranteed by design, not tested in production.

5.3.17. Internal reference voltage characteristics

Table 5-25 Internal reference voltage characteristics

Symbol	Parameter	Minimum	Typical	Maximum	Unit
V_{REFINT}	Internal reference voltage	1.17	1.2	1.23	V
$t_{start\_vrefint}$	Start time of internal reference voltage	-	10	15	us
T_{coeff}	Temperature coefficient	-	-	100(1)	ppm/℃
I_{vcc}	Current consumption from V_{CC}	-	12	20	uA

5.3.18. Timer characteristics

Table 5-26 Timer characteristics

Symbol	Parameter	Condition	Minimum	Maximum	Unit
$t_{res(TIM)}$	Timer resolution time	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 32 MHz	20.833	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4	-	-	$f_{TIMxCLK}$/2	MHz
		$f_{TIMxCLK}$ = 32 MHz	-	24	
Res_{TIM}	Timer resolution	TIM1/3/14/16/17	-	16	Bit
$t_{COUNTER}$	16-bit counter clock period	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 32 MHz	0.020833	1365	us

Table 5-27LPTIM characteristics (clock selection LSI)

Prescaler	PRESC[2:0]	Minimum overflow	Maximum overflow	Unit
/1	0	0.0305	1998.848	ms
/2	1	0.0610	3997.696	
/4	2	0.1221	8001.9456	
/8	3	0.2441	15997.3376	
/16	4	0.4883	32001.2288	
/32	5	0.9766	64002.4576	
/64	6	1.9531	127998.3616	
/128	7	3.9063	256003.2768	

Table 5-28IWDG characteristics (clock selection LSI)

Prescaler	PR[2:0]	Minimum overflow	Maximum overflow	Unit
/4	0	0.122	499.712	ms
/8	1	0.244	999.424	
/16	2	0.488	1998.848	
/32	3	0.976	3997.696	
/64	4	1.952	7995.392	
/128	5	3.904	15990.784	
/256	6 or 7	7.808	31981.568	

Table 5-29 WWDG characteristics (clock select 32 MHz PCLK)

Prescaler	WDGTB[1:0]	Minimum overflow	Maximum overflow value	Unit
1*4096	0	0.085	5.461	ms
2*4096	1	0.171	10.923	
4*4096	2	0.341	21.845	
8*4096	3	0.683	43.691	

5.3.19. Communication port characteristics

5.3.19.1. I²C bus interface features

I²C interface meets the requirements of the I²C -bus specification and user manual :

- Standard-mode(Sm): 100 kbit/s
- Fast-mode(Fm): 400 kbit/s

Timing is guaranteed by design, provided the I²C peripheral is properly configured and the I²C CLK frequency is greater than the minimum required in the table below.

Table 5-30 Minimum I²C CLK frequency

Symbol	Parameter	Condition	Minimum	Unit
$f_{I2CCLK(min)}$	Minimum I²C CLK freq uency	Standard-mode	2	MHz
		Fast-mode	9	

I²C SDA and SCL pins have analog filtering, see table below.

Table 5-31 I²C filter characteristics

Symbol	Parameter	Minimum	Maximum	Unit
t_{AF}	Limiting duration of spikes suppressed by the filter (Spik-ers shorter than the limiting duration are suppressed)	50	260	ns

5.3.19.2. Serial Peripheral Interface SPI Characteristics

Table 5-32 SPI characteristics

Symbol	Parameter	Condition	Minimum	Maximum	Unit
f_{SCK}		Master mode	-	12	MHz

Symbol	Parameter	Condition	Minimum	Maximum	Unit
$1/t_{c(SCK)}$	SPI clock frequency	Slave mode	-	12	
$t_{r(SCK)}$ $t_{f(SCK)}$	SPI clock rise and fall time	Capacitive load: C=15 pF	-	6	ns
$t_{su(NSS)}$	NSS setup time	Slave mode	4Tpclk	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode	2Tpclk + 10	-	ns
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high and low time	Master mode,presc = 4	Tpclk*2 -2	Tpclk*2 + 1	ns
$t_{su(MI)}$ $t_{su(SI)}$	Data input setup time	Master mode,presc = 4	Tpclk+5(1)	-	ns
		Slave mode, presc = 4	5	-	
$t_{h(MI)}$	Data input hold time	Master mode	5	-	ns
$t_{h(SI)}$		Slave mode	Tpclk+5	-	
$t_{a(SO)}$	Data output access time	Slave mode, presc = 4	0	3Tpclk	ns
$t_{dis(SO)}$	Data output disable time	Slave mode	2Tpclk+5	4Tpclk+5	ns
$t_{v(SO)}$	Data output valid ime	Slave mode (after enable edge)，presc = 4	0	1.5Tpclk(2)	ns
$t_{v(MO)}$	Data output valid ime	Master mode (after enable edge)	-	6	ns
$t_{h(SO)}$	Data output hold time	Slave mode，presc = 4	0(3)	-	ns
$t_{h(MO)}$		Master mode	2	-	
DuCy(SCK)	SPI slave input clock duty cycle	Slave mode	45	55	%

1. The Master generates 1 pclk to receive control signal before the receive edge.
2. Slave has a maximum of 1 PCLK based on the sending edge of SCK delay, considering IO delay, etc., define 1.5 PCLK.
3. In the case that the SCK duty cycle sent by the Master is wide between the receiving edge and the sending edge, the Slave updates the data before the sending edge.

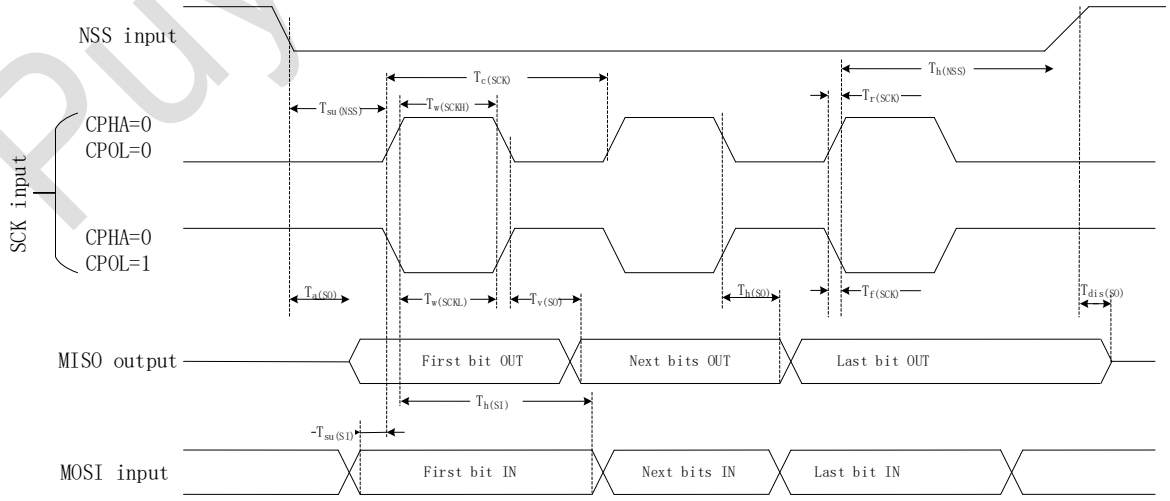


Figure 5-2 SPI timing diagram – slave mode and CPHA=0

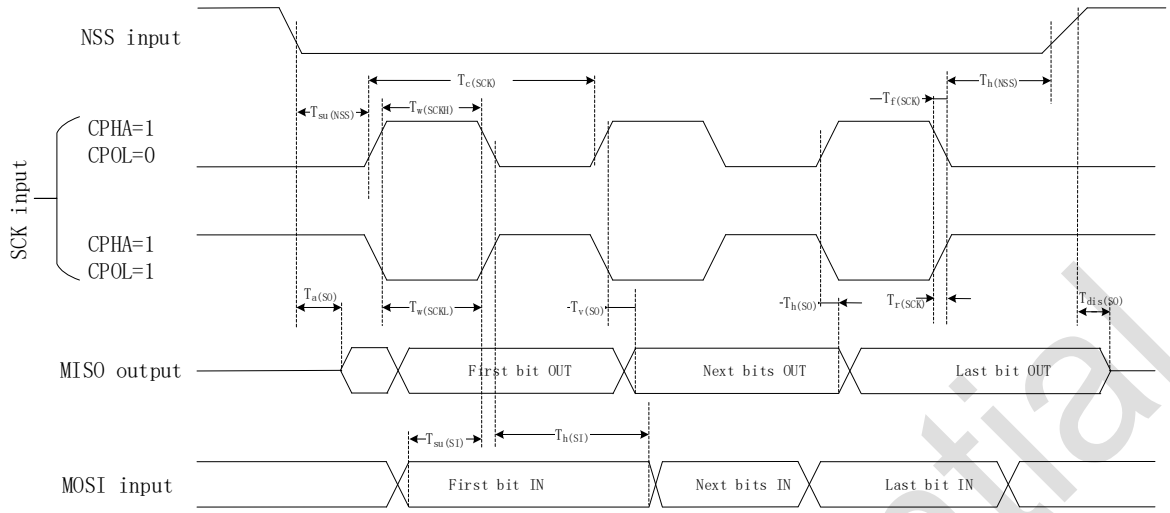


Figure 5-3 SPI timing diagram – slave mode and CPHA=1

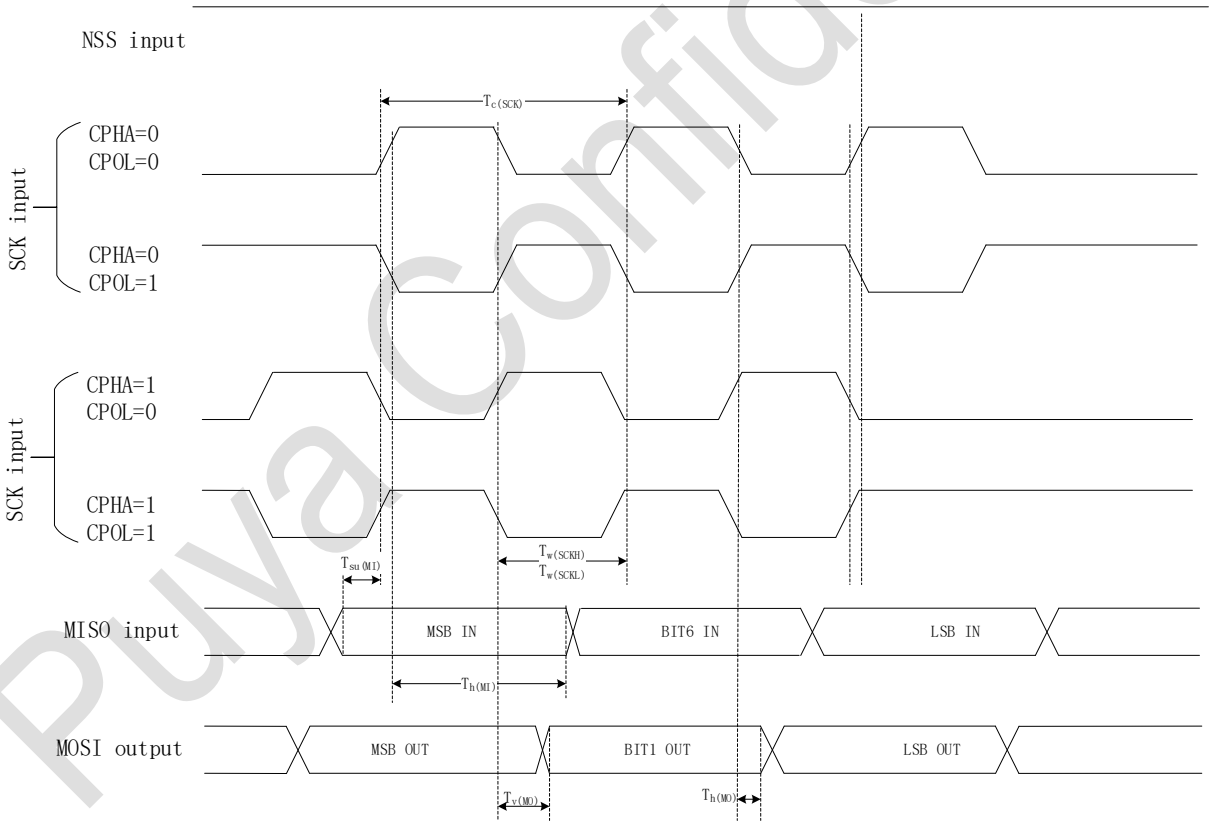


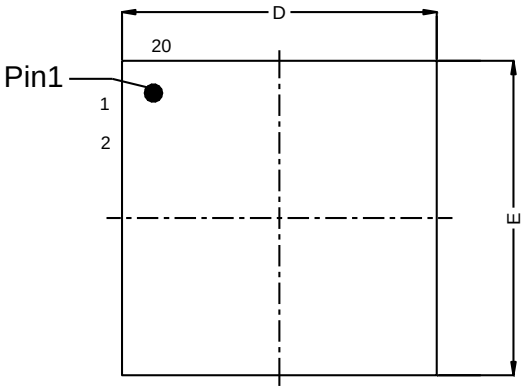
Figure 5-4 SPI timing diagram – master mode

6. Package information

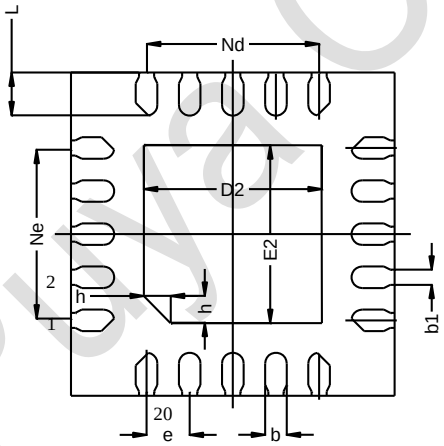
6.1. QFN20

TOP VIEW

SIDE VIEW



BOTTOM VIEW



Common Dimensions

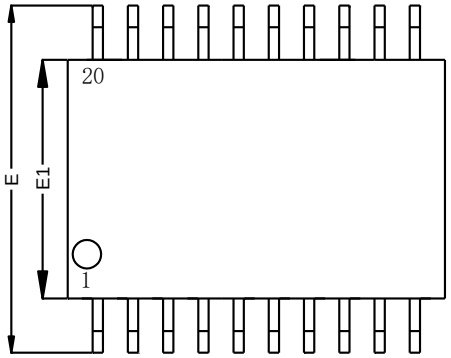
(Unit of Measure=millimeters)

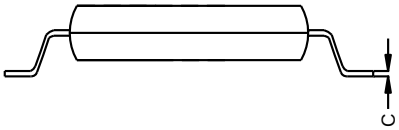
Symbol	Min	Typ	Max
A	0.500	0.550	0.600
A1	0.000	0.020	0.050
b	0.150	0.200	0.250
b1		0.140REF	
c		0.150REF	
D	2.900	3.000	3.100
D2	1.550	1.650	1.750
E	2.900	3.000	3.100
E2	1.550	1.650	1.750
e		0.400BSC	
Nd		1.600BSC	
Ne		1.600BSC	
L	0.350	0.400	0.450
h	0.200	0.250	0.300

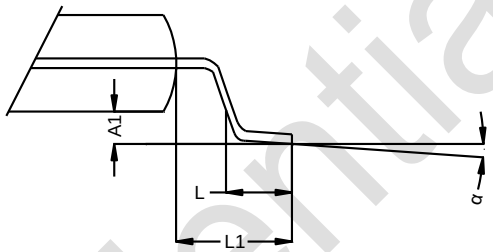
Note：1. Dimensions are not to scale

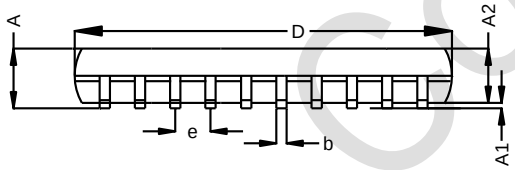
	TITLE	DRAWING NO.	REV
PUYA	Puya QFN20L 3x3X0.55-0.4PITCH POD	QRPD-0041	1.0

6.2. TSSOP20









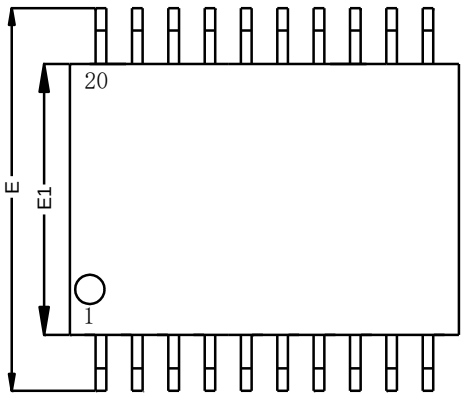
Common Dimensions
(Unit of Measure=millimeters)

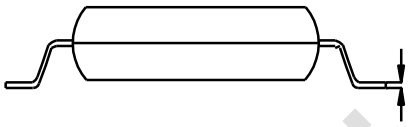
Symbol	Min	Typ	Max
A	-	-	1.200
A1	0.050	-	0.150
A2	0.800	1.000	1.050
b	0.200	-	0.280
c	0.090	-	0.200
D	6.400	6.500	6.600
E	6.200	6.400	6.600
E1	4.300	4.400	4.500
e	0.650BSC		
L	0.450	0.600	0.750
L1	1.000REF		
θ	0	-	8°

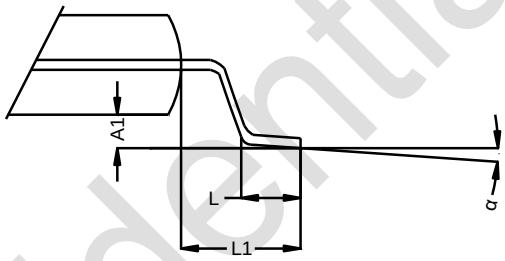
Note：1. Dimensions are not to scale

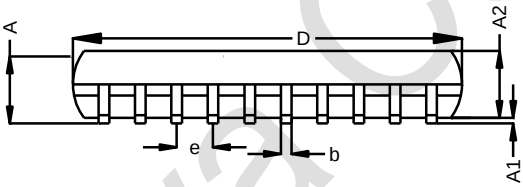
	TITLE	DRAWING NO.	REV
PUYA	Puya TSSOP20 POD	QRPD-0043	1.0

6.3. SOP20









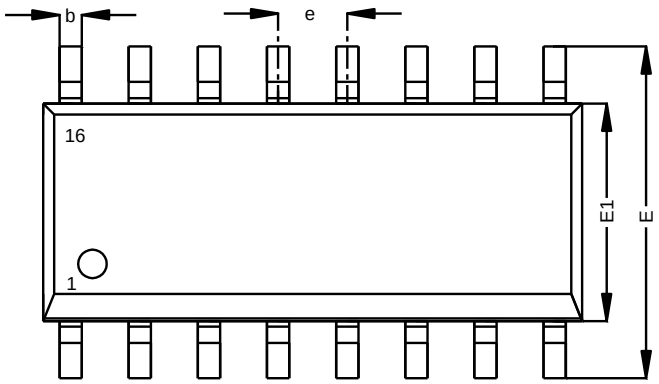
Common Dimensions
(Unit of Measure=millimeters)

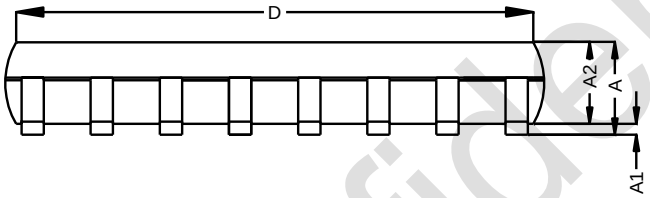
Symbol	Min	Typ	Max
A	-	-	2.650
A1	0.100	-	0.300
A2	2.100	2.300	2.500
b	0.330	-	0.510
c	0.200	-	0.330
D	12.600	12.800	13.000
E	10.100	10.300	10.500
E1	7.400	7.500	7.600
e	1.275BSC		
h	0.300	-	0.500
L	0.400	-	1.270
L1		1.400REF	
θ	0	-	8°

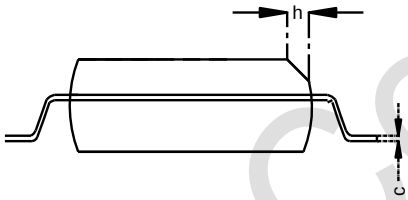
Note：1. Dimensions are not to scale

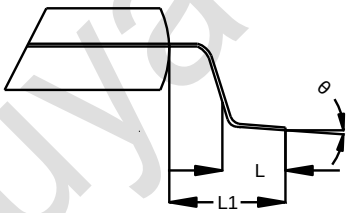
	TITLE	DRAWING NO.	REV
PUYA	Puya SOP20 POD	QRPD-0048	1.0

6.4. SOP16









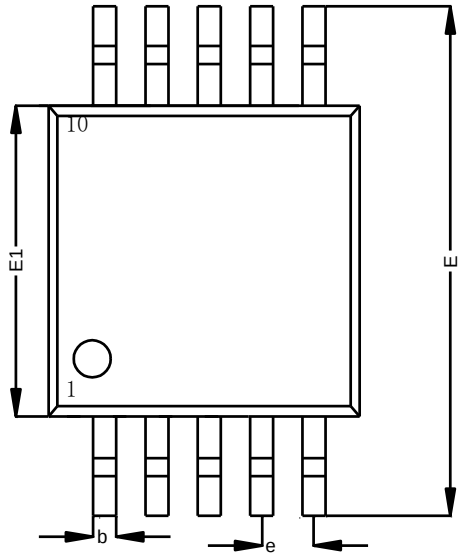
Common Dimensions
(Unit of Measure=millimeters)

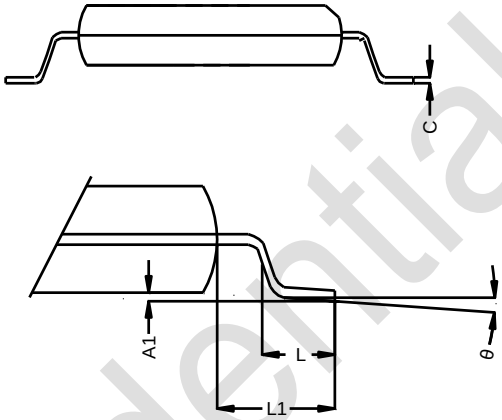
Symbol	Min	Typ	Max
A	-	-	1.75
A1	0.10	-	0.25
A2	1.30	-	-
b	0.31	-	0.51
c	0.10	-	0.25
D	9.80	-	10.20
E	5.80	-	6.20
E1	3.80	-	4.20
e	1.27BSC		
L	0.40	-	1.27
L1	1.05REF		
θ	0	-	8°
h	0.25	-	0.50

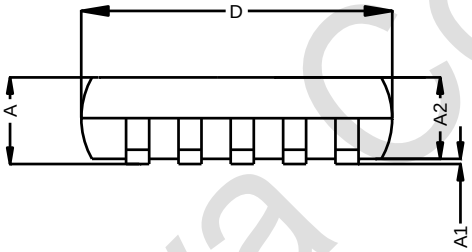
Note: Dimensions are not to scale.

	TITLE	DRAWING NO.	REV
PUYA	PUYA SOP16 (150mil) POD	QRPD-0001	1.1

6.5. MSOP10







Common Dimensions

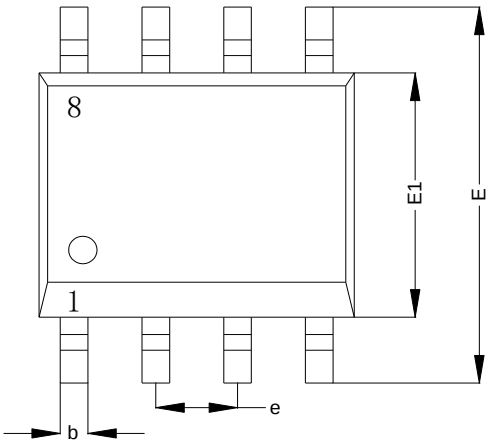
(Unit of Measure=millimeters)

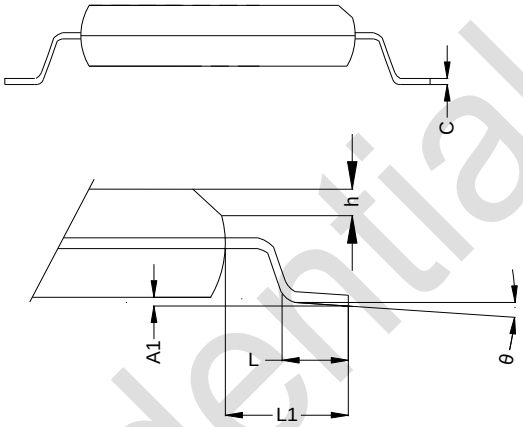
Symbol	Min	Typ	Max
A	-	-	1.100
A1	0.050	-	0.150
A2	0.750	0.850	0.950
b	0.180	-	0.270
c	0.150	-	0.200
D	2.900	3.000	3.100
E	4.700	4.900	5.100
E1	2.900	3.000	3.100
e	-	0.500	-
L	0.400	-	0.700
L1	-	0.950	-
θ	0	-	8°

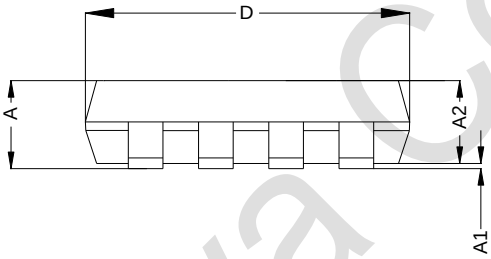
Note：1. Dimensions are not to scale

	TITLE	DRAWING NO.	REV
PUYA	Puya MSOP10 POD	QRPD-0049	1.0

6.6. SOP8







Common Dimensions

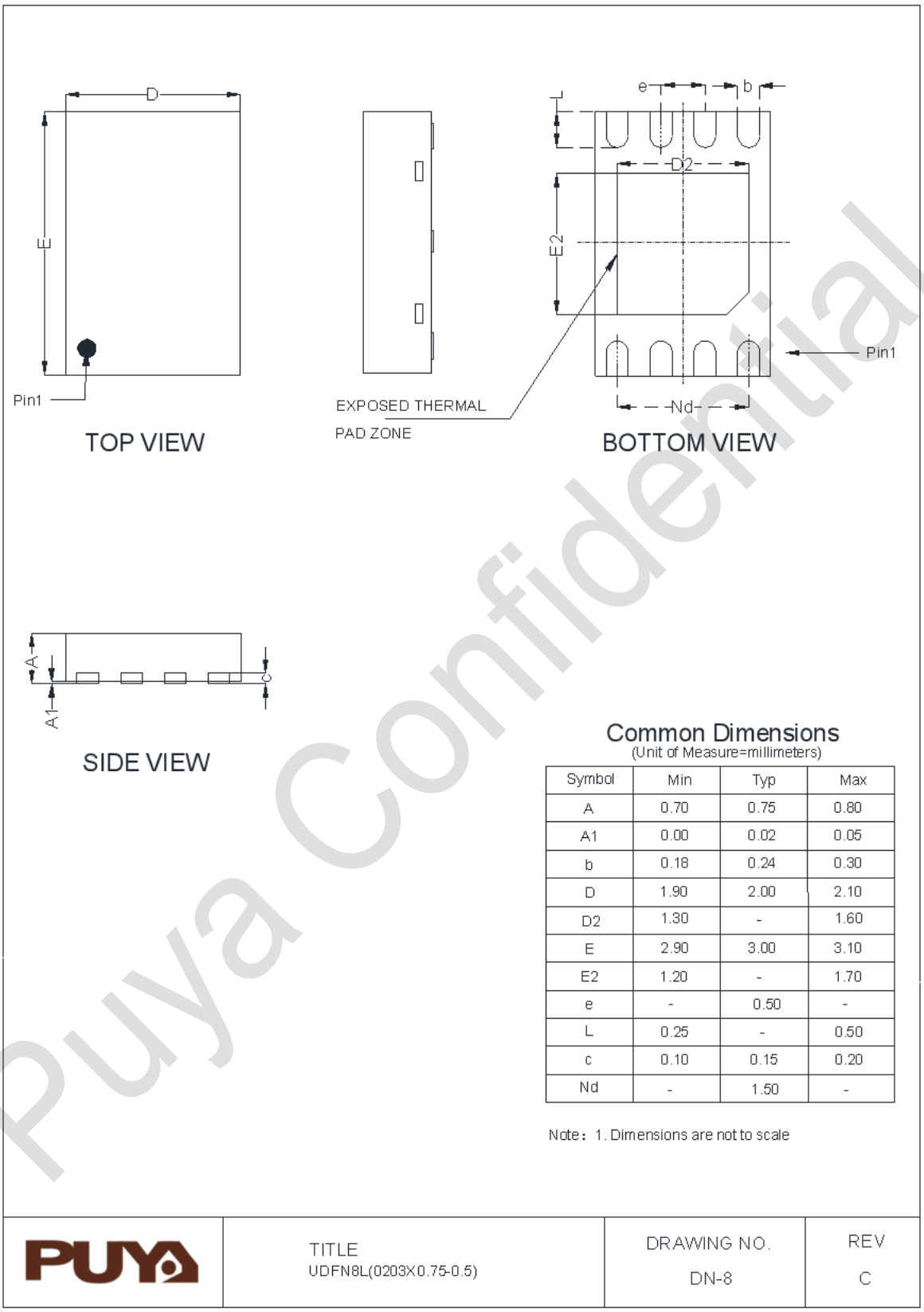
(Unit of Measure=millimeters)

Symbol	Min	Typ	Max
A	1.350	-	1.750
A1	0.100	-	0.250
A2	1.250	-	-
b	0.310	-	0.510
c	0.170	-	0.250
D	4.800	4.900	5.000
E	5.800	6.000	6.200
E1	3.800	3.900	4.000
e	-	1.270	-
L	0.400	-	1.270
L1	-	1.050	-
θ	0	-	8°
h	0.25	-	0.50

Note：1. Dimensions are not to scale

	TITLE	DRAWING NO.	REV
PUYA	Puya SOP8（150mil）POD	QRPD-0004	1.1

6.7. DFN8(3*2)



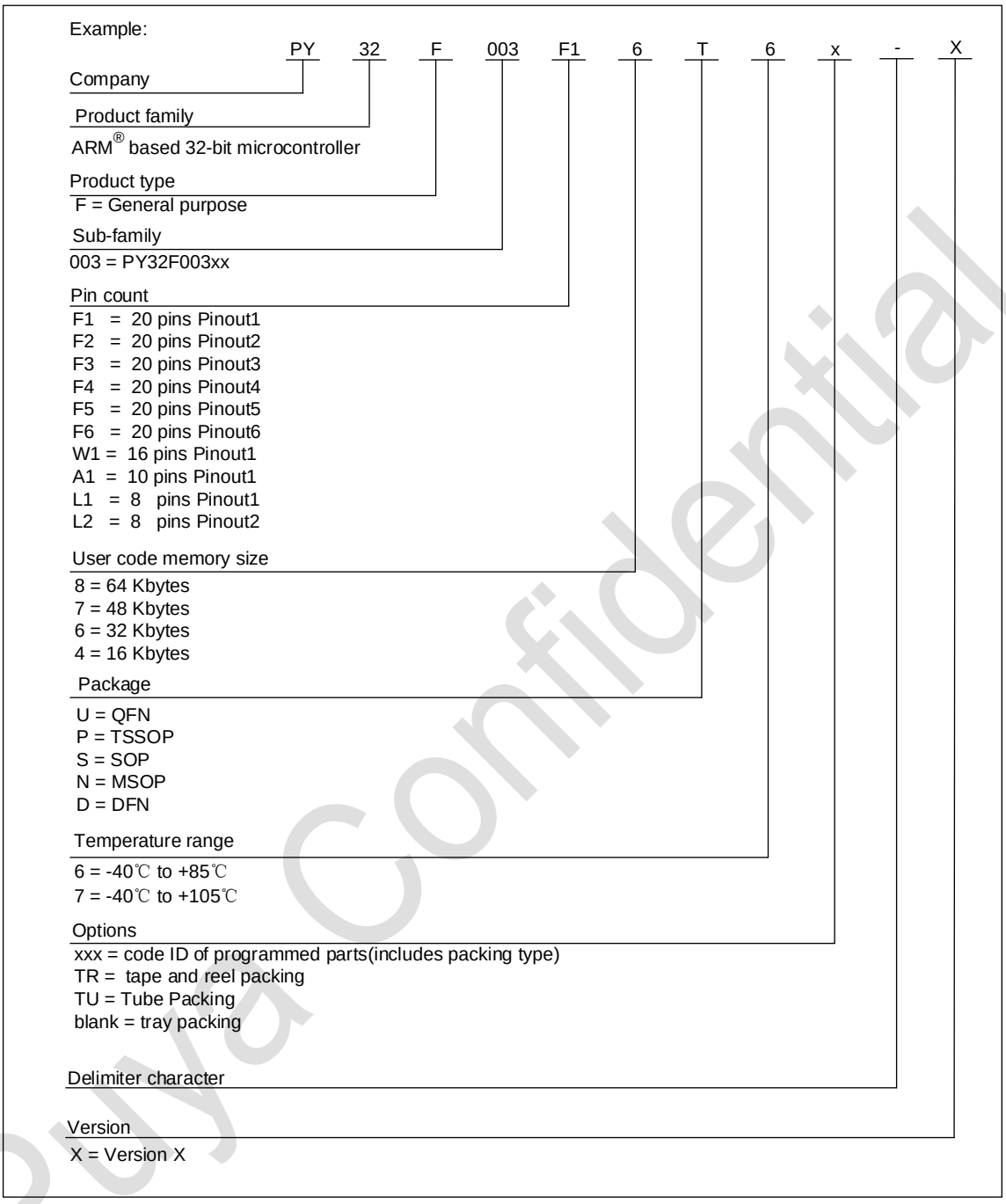
Common Dimensions
(Unit of Measure=millimeters)

Symbol	Min	Typ	Max
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
b	0.18	0.24	0.30
D	1.90	2.00	2.10
D2	1.30	-	1.60
E	2.90	3.00	3.10
E2	1.20	-	1.70
e	-	0.50	-
L	0.25	-	0.50
c	0.10	0.15	0.20
Nd	-	1.50	-

Note：1. Dimensions are not to scale

	TITLE	DRAWING NO.	REV
PUYA	UDFN8L(0203X0.75-0.5)	DN-8	C

7. Ordering Information



8. Version history

Version	Date	Description
V1.0	2022-01-14	Initial version
V1.1	2022-01-18	1. Updated Table 2-1 2. Updated Table 6-15
V1.2	2022-01-24	1. Updated parameters in Table 6-30
V1.3	2023-01-24	1. Updated the format
V1.4	2024-02-06	1. Add SOP20/SOP16/MSOP10/DFN8(3*2) /SOP8 packages
V1.5	2024-02-23	1. Add PY32F003F16U6-E(QFN20 package)
V1.6	2024-03-13	1. Add PY32F003F16P6-E/PY32F003F18U7-E
V1.7	2024-05-16	1. Add PY32F003F68P7-E (TSSOP20 package)

Puya Semiconductor Co., Ltd.